



H57H-AM2

V : 2.0

SCHEMATICS TABLE:


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20	PCH PWR RAILS,Decoupling
21	PCH GND Pins
22	PCH Video and DDSP
23	PCH CLOCKS,Straps

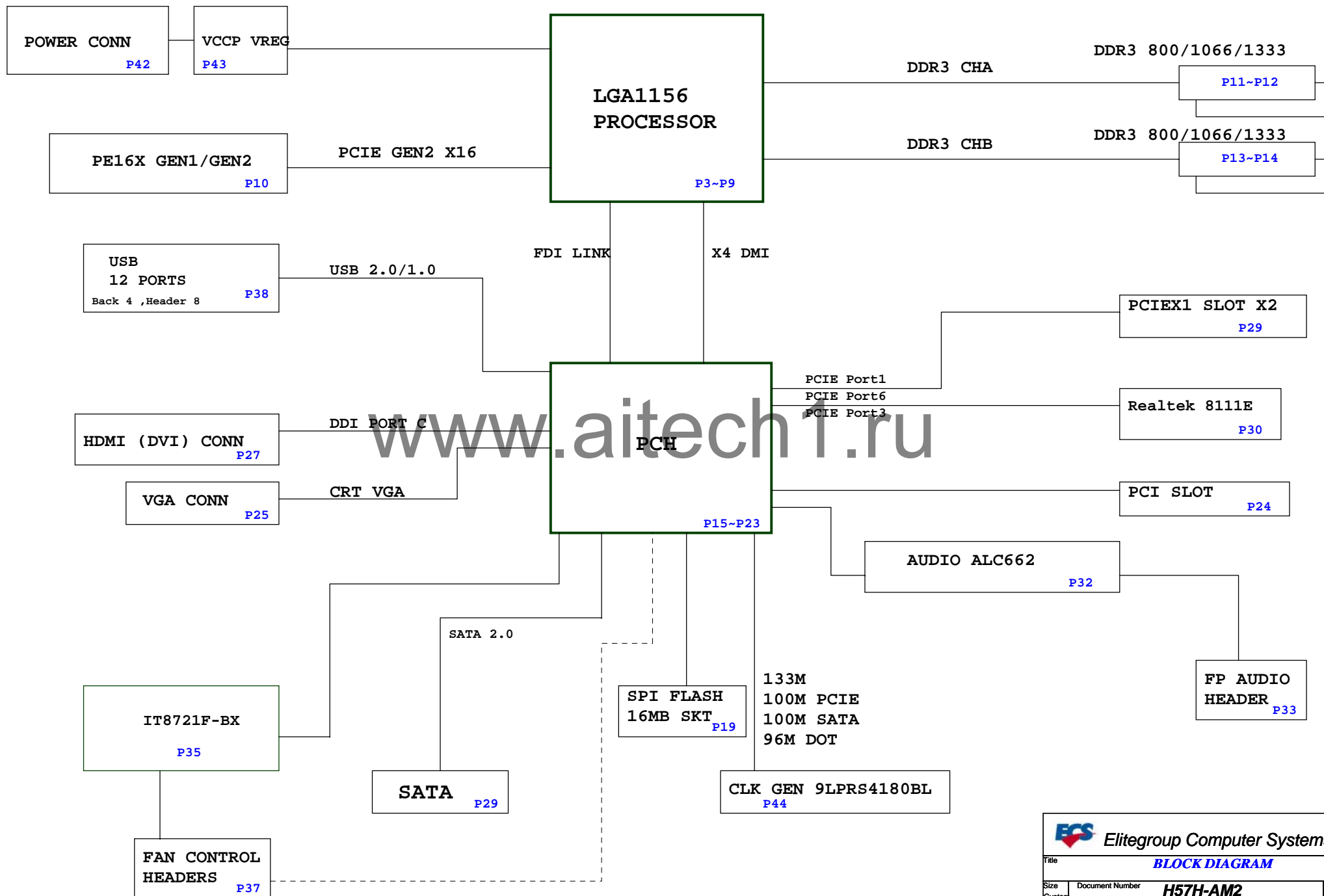
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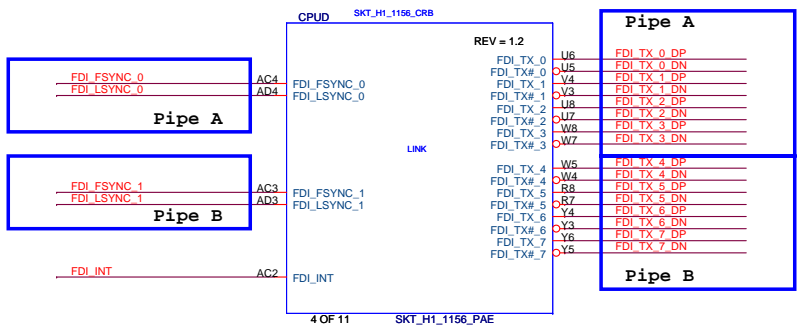
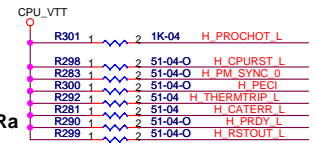
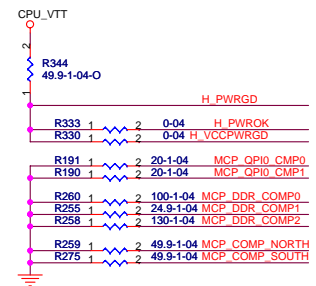
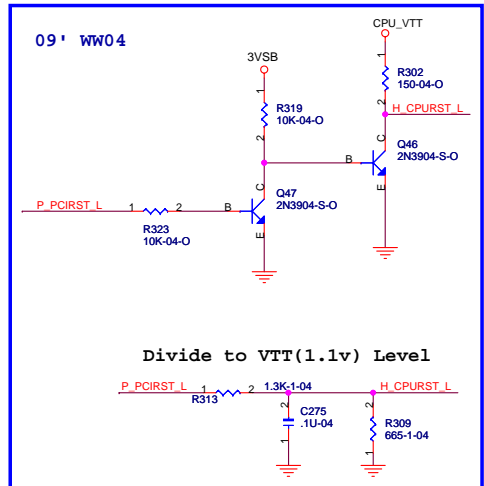
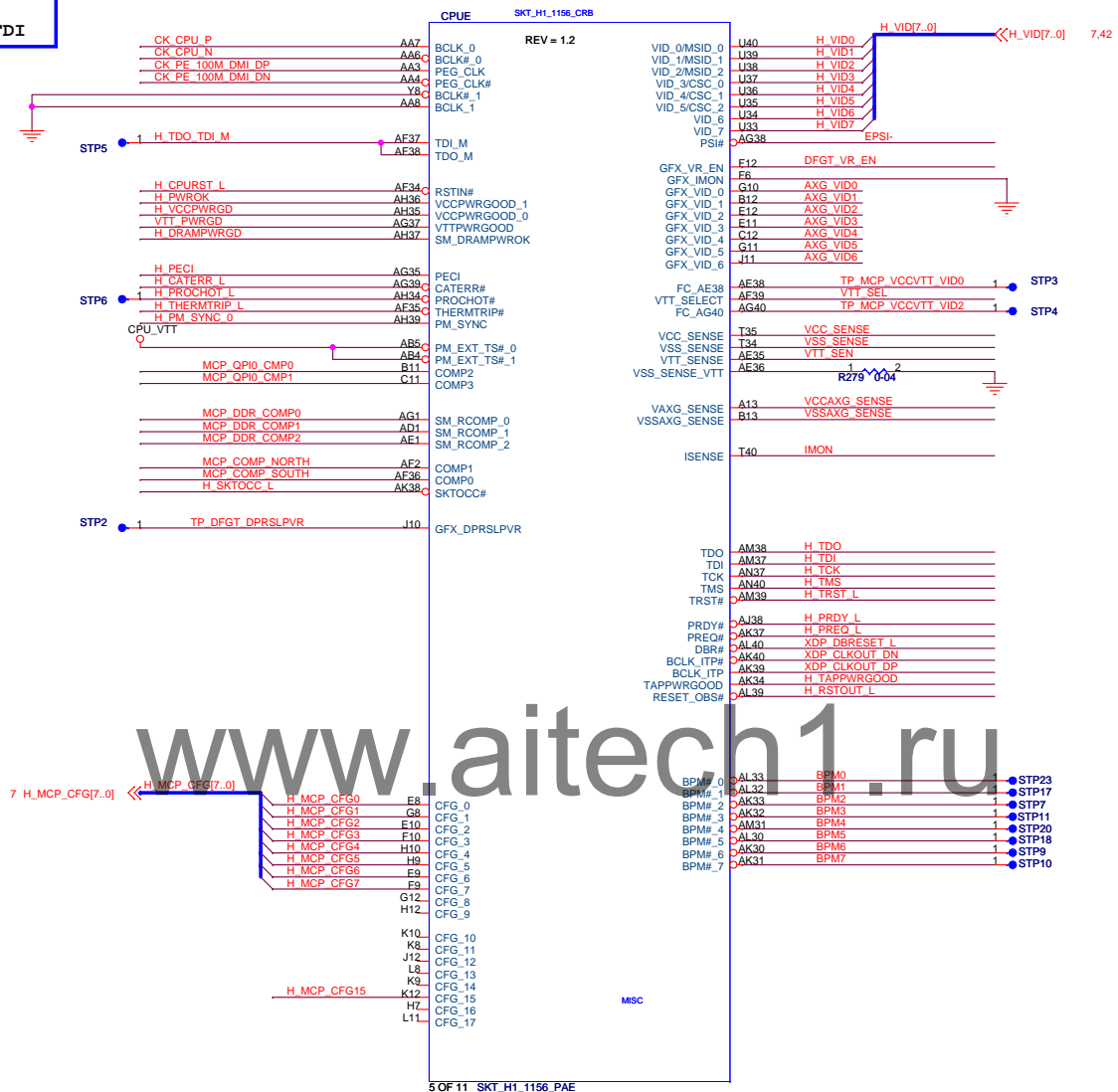
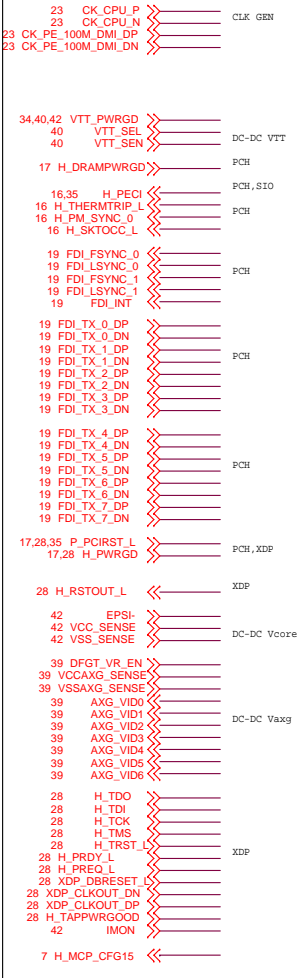
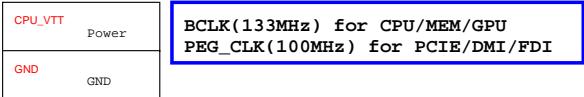
REVISION HISTORY:

Rev	Date	Notes
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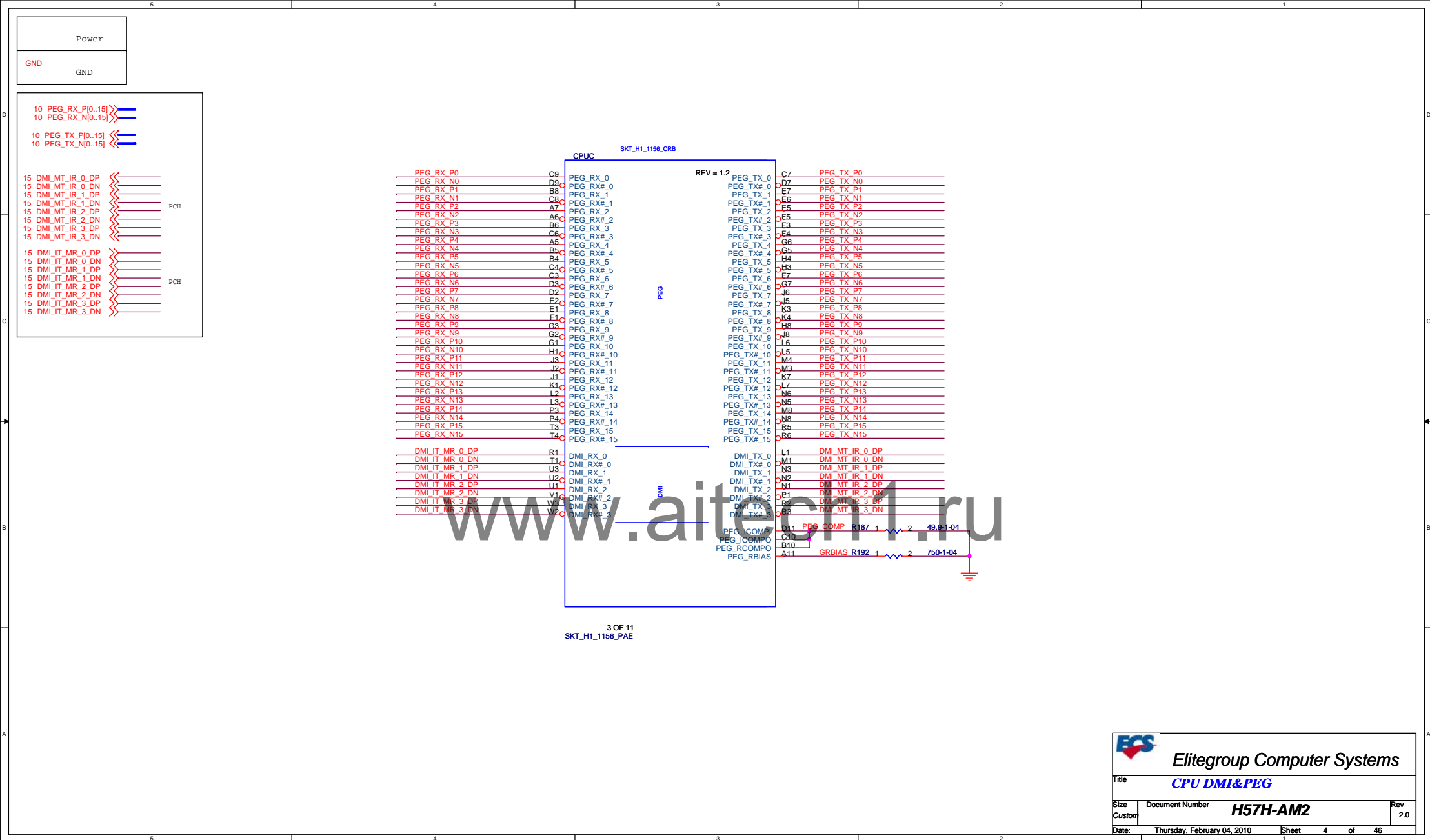
@ ECS
CONFIDENTIAL @

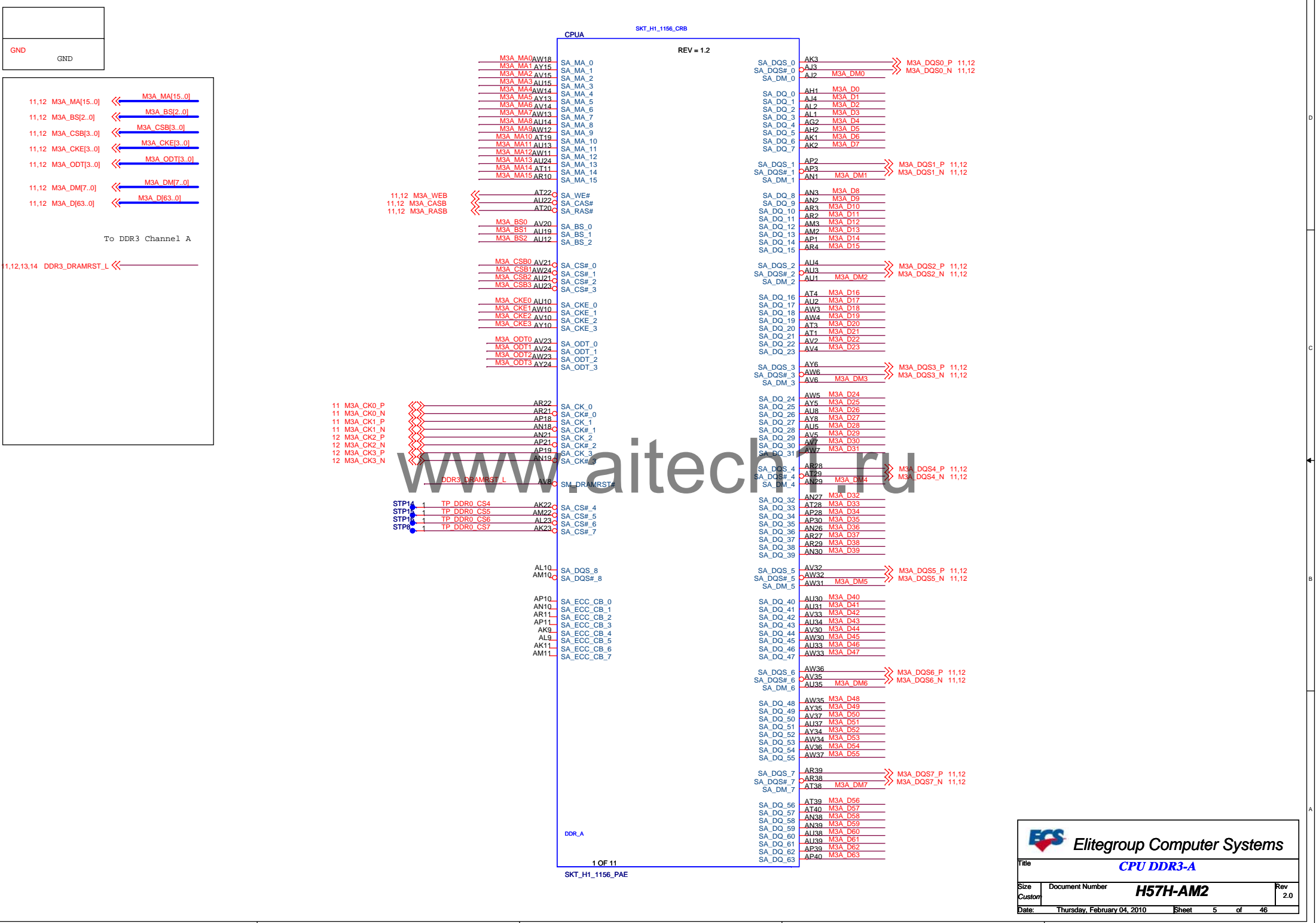
 Elitegroup Computer Systems	
Title Cover Page	
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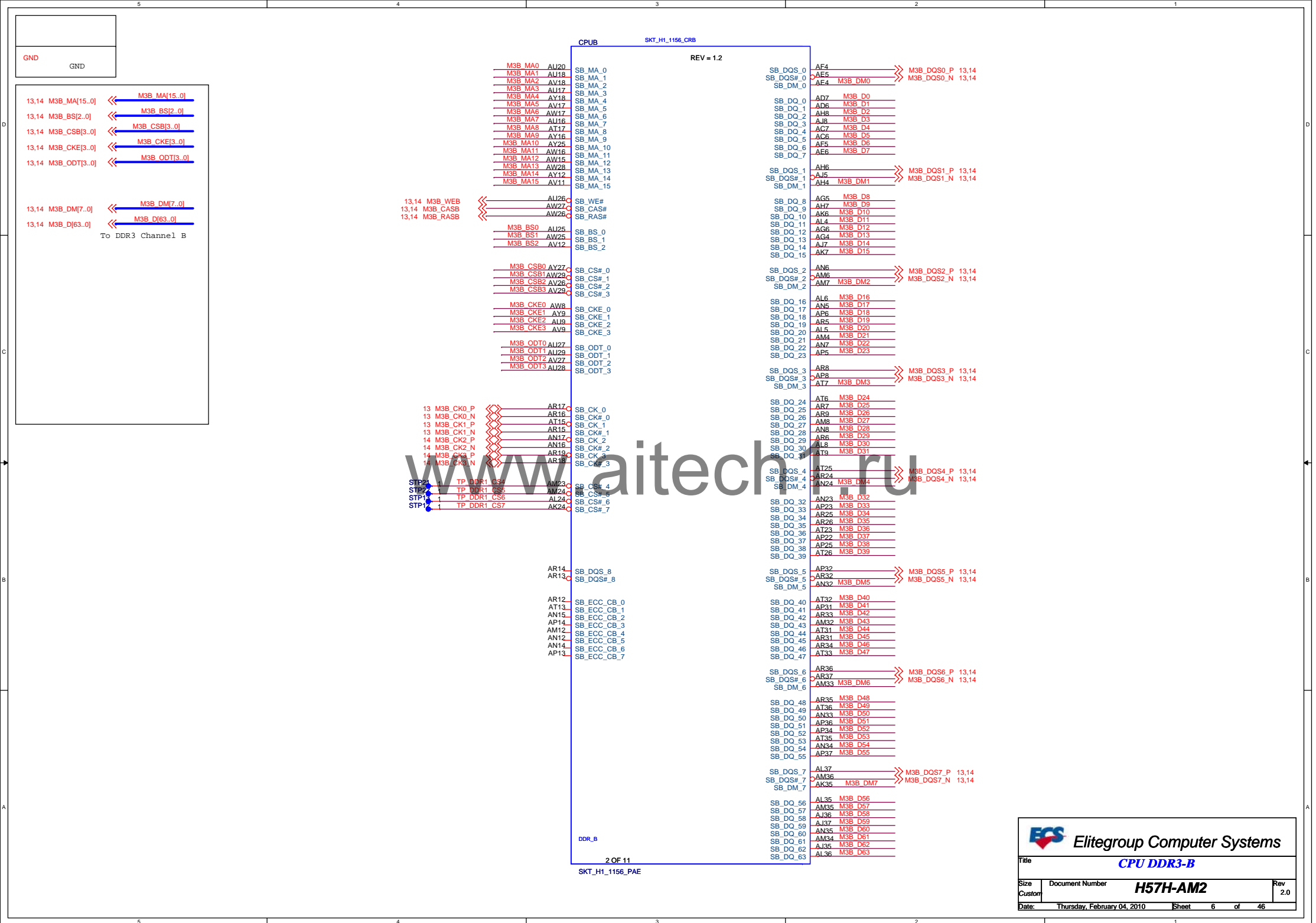




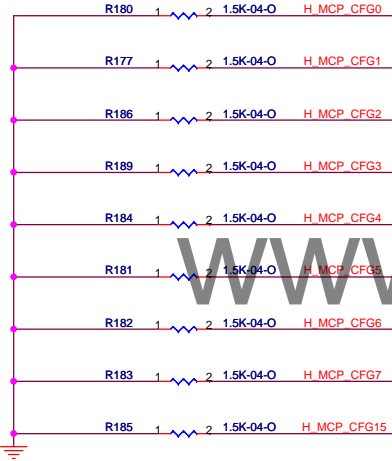
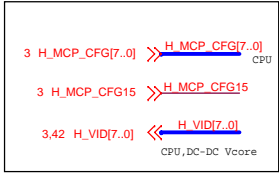
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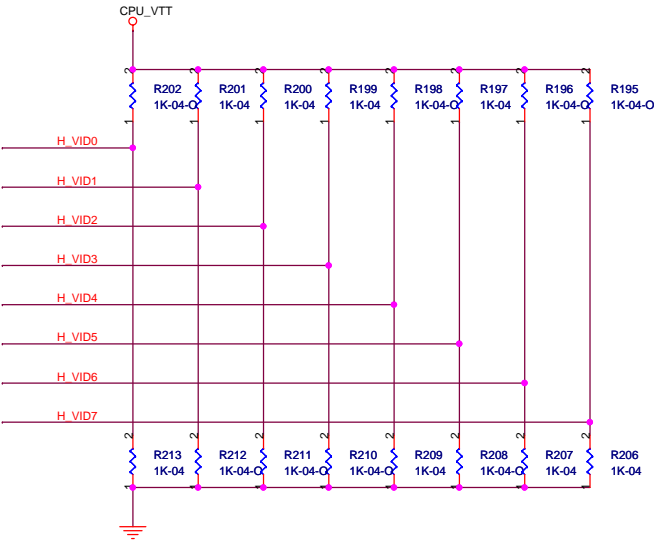


CPU_VTT	Power
GND	GND



CFG(1:0)
Desktop
11 PCIE16X
10 PCIE18X
CFG2,4,5,6,7~17
Reserved configuration land
CFG3
Havendale PCIE static Lan Numbering reversal

CFG	Havendale	Lynnfield			
0	REVERSED	1	11=1*16X	0	10=2*8X
1	REVERSED	1		1	
2	REVERSED			REVERSED	
3	Static Lane Number Reversal			REVERSED	
4	REVERSED			REVERSED	
6	REVERSED				
7	REVERSED				
15	REVERSED				
0,1,2,3,4,5 ALL HAVE INTERNAL PULL-UPS					



POWER ON CONFIGURATION (POC)TABLE

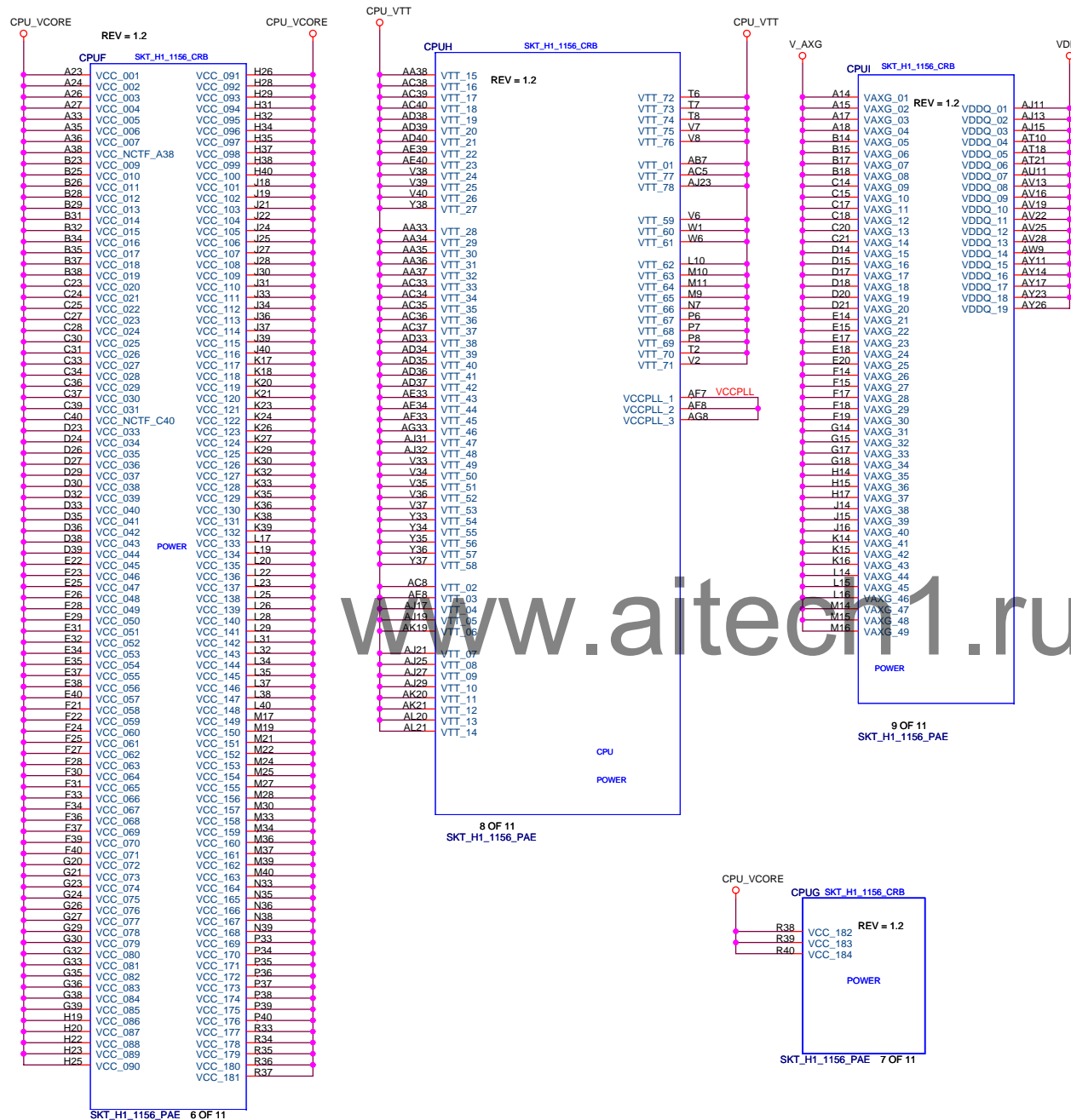
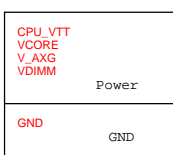
	FUNCTION	Setting	Havendale	Lynnfield
VID0	MIS0	0	Support	Support
VID1	MIS1	1		
VID2	MIS2	1		
VID3	IMON CONFIG CSC0	1	Icc(MAX)=120A	Icc(MAX)=120A
VID4	IMON CONFIG CSC1	0		
VID5	IMON CONFIG CSC2	1		
VID6	RESERVED	0		
VID7	VID SELECT	0		
PSI#	RESERVED	LOW		

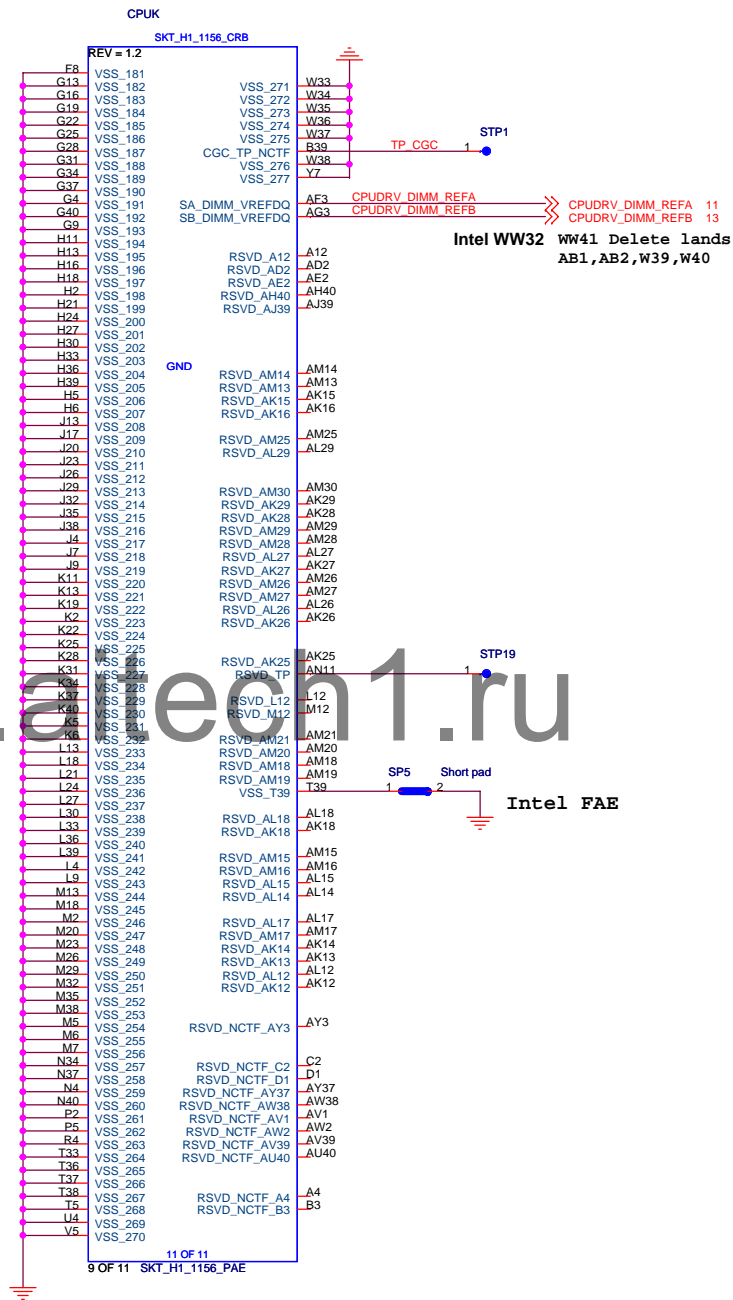
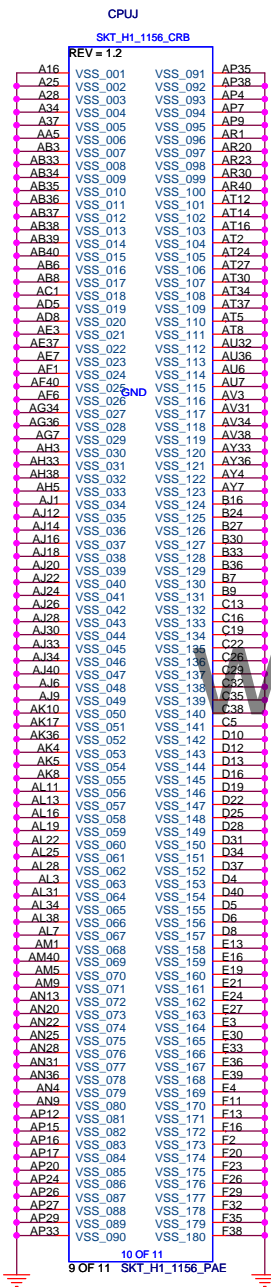
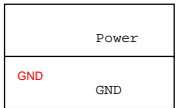
*MSID(2:0)
110 Lynnfield and Havendale support
*CSC(0:2)
Iout Gain and POC setting
100 ICC(max) 80A~100A
101 ICC(max) 100A~120A
110 ICC(max) 120A~140A

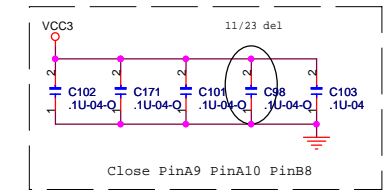
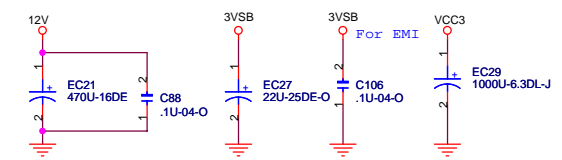
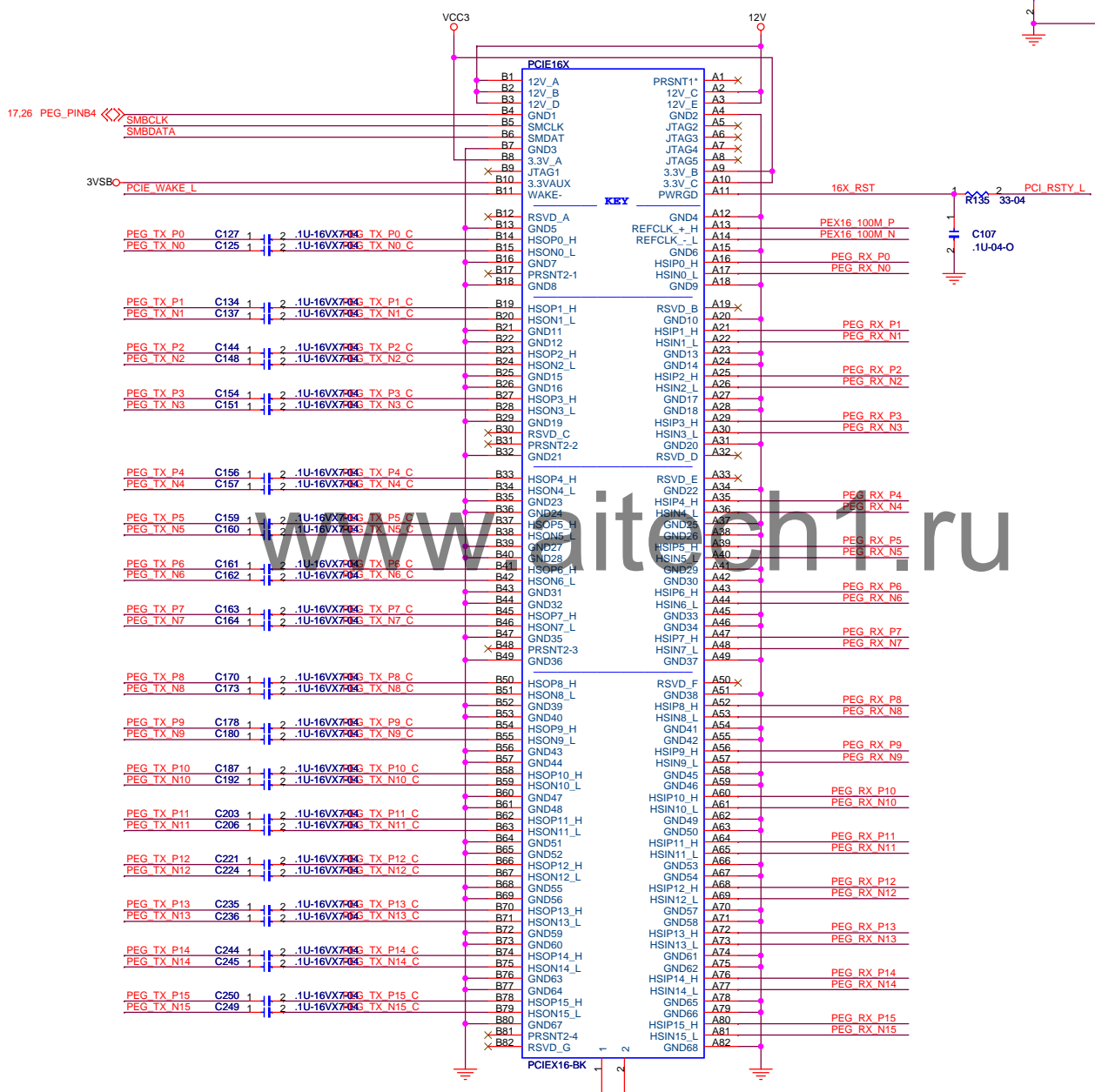
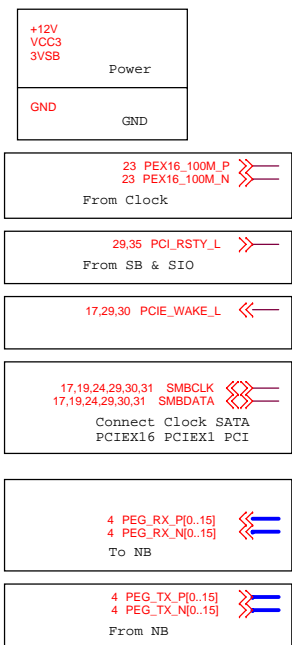


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Title	CPU CFG		
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5,12 M3A_DQS7_N
5,12 M3A_DQS7_P
5,12 M3A_DQS6_N
5,12 M3A_DQS6_P
5,12 M3A_DQS5_N
5,12 M3A_DQS5_P
5,12 M3A_DQS4_N
5,12 M3A_DQS4_P
5,12 M3A_DQS3_N
5,12 M3A_DQS3_P
5,12 M3A_DQS2_N
5,12 M3A_DQS2_P
5,12 M3A_DQS1_N
5,12 M3A_DQS1_P
5,12 M3A_DQS0_N
5,12 M3A_DQS0_P

M3A_ODT0
M3A_ODT1

RSVD
ODT0
NC/PAIR IN
NC/FERR OUT
NC/TEST4

198 FREE1
187 FREE2
48 FREE3
48 FREE4
240 VTT1
239 VSS
238 VSS
237 VSS
228 VSS
227 VSS
226 VSS
225 VSS
224 VSS
223 VSS
222 VSS
221 VSS
217 VSS
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9 VSS
8 VSS
7 VSS
6 VSS
5 VSS
4 VSS
3 VSS
2 VSS
1 VSS

CHANNEL A DIMM0

5,12 M3A_DM[7..0]

M3A_DM0
M3A_DM1
M3A_DM2
M3A_DM3
M3A_DM4
M3A_DM5
M3A_DM6
M3A_DM7

DM0DQS9
DM1DQS10
DM2DQS11
DM3DQS12
DM4DQS13
DM5DQS14
DM6DQS15
DM7DQS16
DM8DQS17
NC/DQS9
NC/DQS10
NC/DQS11
NC/DQS12
NC/DQS13
NC/DQS14
NC/DQS15
NC/DQS16
NC/DQS17

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M3A_D62
M3A_D63

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DO(63)

DDR3-240P-BL

M3A_WEB 5,12
M3A_RASB 5,12
M3A_CASB 5,12

DDR3_DRAMRST_L 5,12,13,14

M3A_MA[15..0] 5,12

M3A_CK0_P 5
M3A_CK0_N 5
M3A_CK1_P 5
M3A_CK1_N 5

M3A_ODT[3..0] 5,12
M3A_CSB[3..0] 5,12
M3A_CKE[3..0] 5,12
M3A_BS[2..0] 5,12

12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

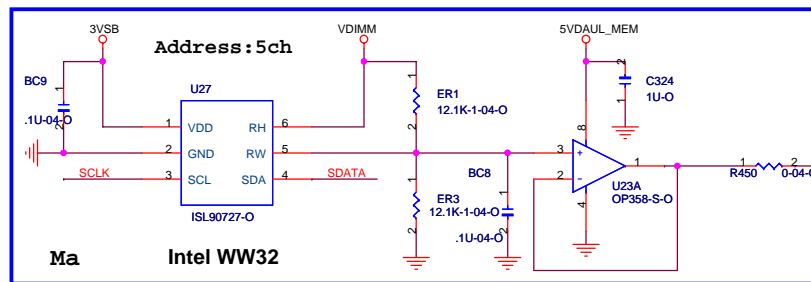
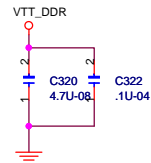
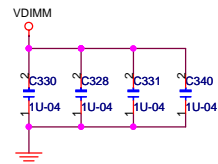
12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

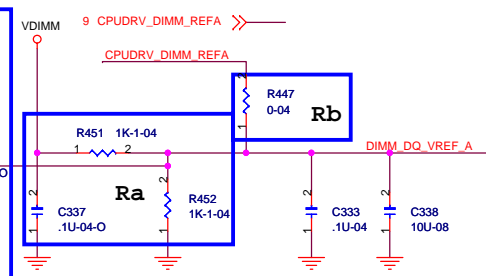
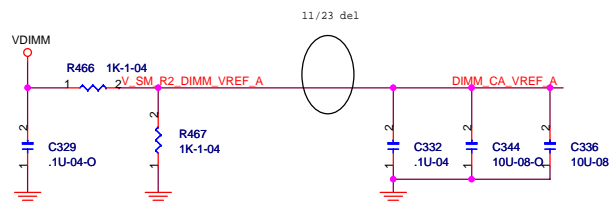
12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

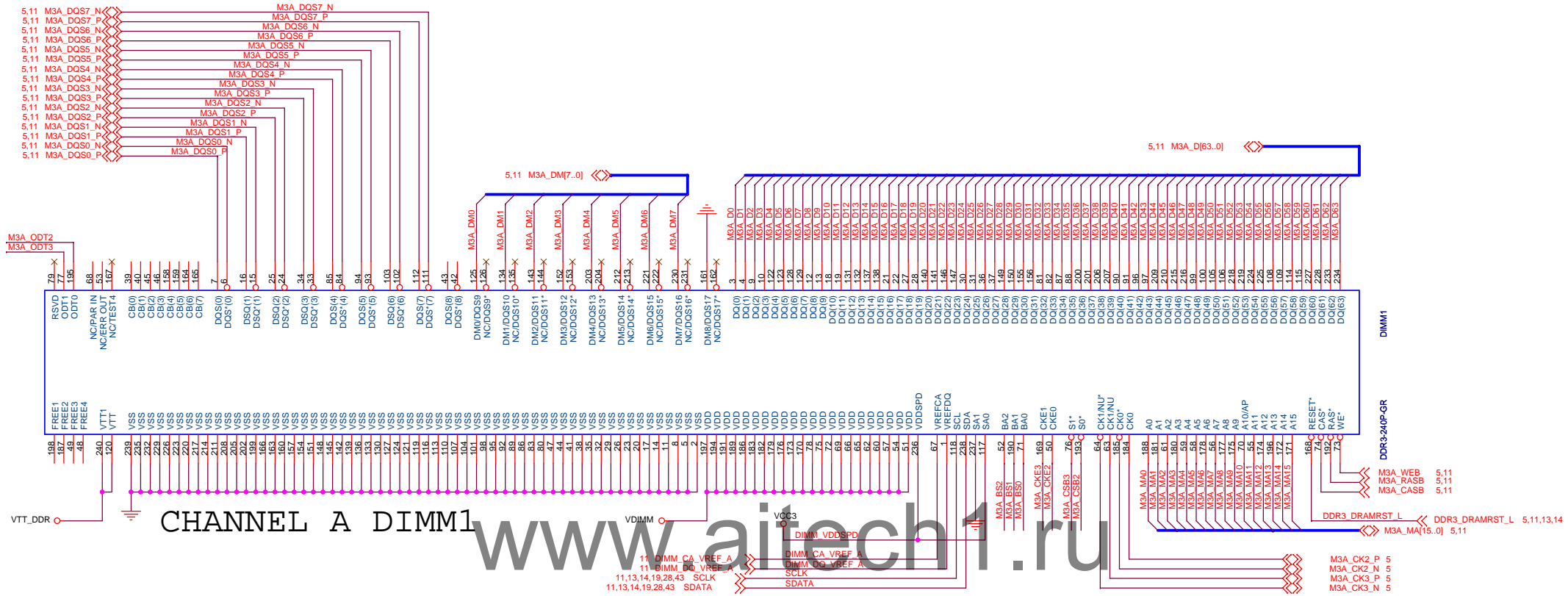
12,13,14,19,28,43 SCLK
12,13,14,19,28,43 SDATA

DG0.8:1u-04*4 For VDIMM
4.7u*1+0.1u*4 For DDR_VTT
Per DIMM



DQ_VREF Control Mode	
Mode 1	Ra
Mode 2	Rb
Mode 3	Ma Ra=2.2OHM

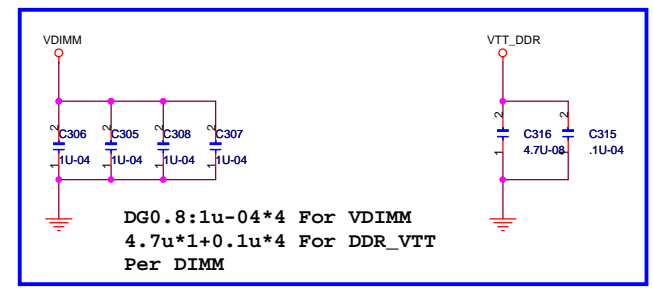





CHANNEL A DIMM1

www.aitech1.ru

DDR_VTT	Power
VDIMM	
DIMM_VDDSPD	
GND	GND



**Elitegroup Computer Systems**

Title

CONN DDR3, CH A DIMM1

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6.13 M3B_DQS7_N
6.13 M3B_DQS7_P
6.13 M3B_DQS6_N
6.13 M3B_DQS6_P
6.13 M3B_DQS5_N
6.13 M3B_DQS5_P
6.13 M3B_DQS4_N
6.13 M3B_DQS4_P
6.13 M3B_DQS3_N
6.13 M3B_DQS3_P
6.13 M3B_DQS2_N
6.13 M3B_DQS2_P
6.13 M3B_DQS1_N
6.13 M3B_DQS1_P
6.13 M3B_DQS0_N
6.13 M3B_DQS0_P

M3B_ODT2
M3B_ODT3

6.13 M3B_DM[7..0]

6.13 M3B_D[63..0]

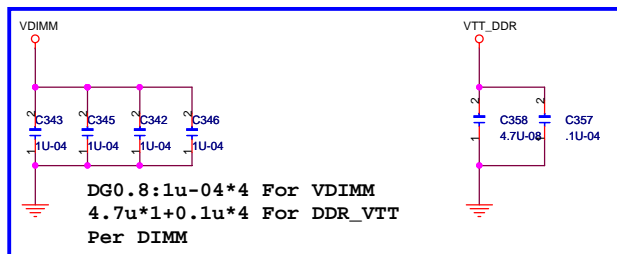
CHANNEL B DIMM1

13 DIMM_CA_VREF_B
13 DIMM_DQ_VREF_B
11,12,13,19,28,43 SCLK
11,12,13,19,28,43 SDATA

DIMM_CA_VREF_B
DIMM_DQ_VREF_B
SCLK
SDATA

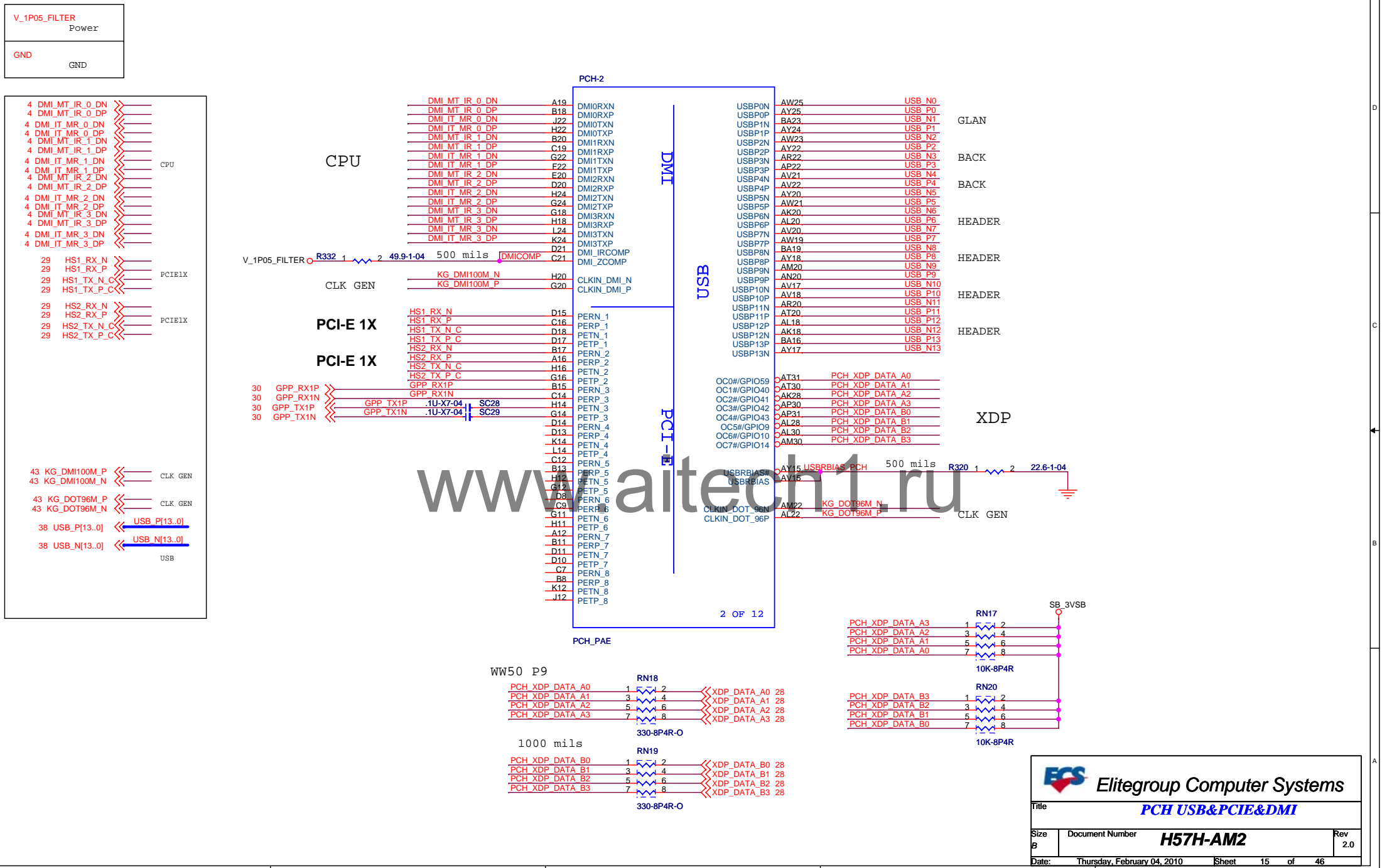
M3B_CK2_P 6
M3B_CK2_N 6
M3B_CK3_P 6
M3B_CK3_N 6

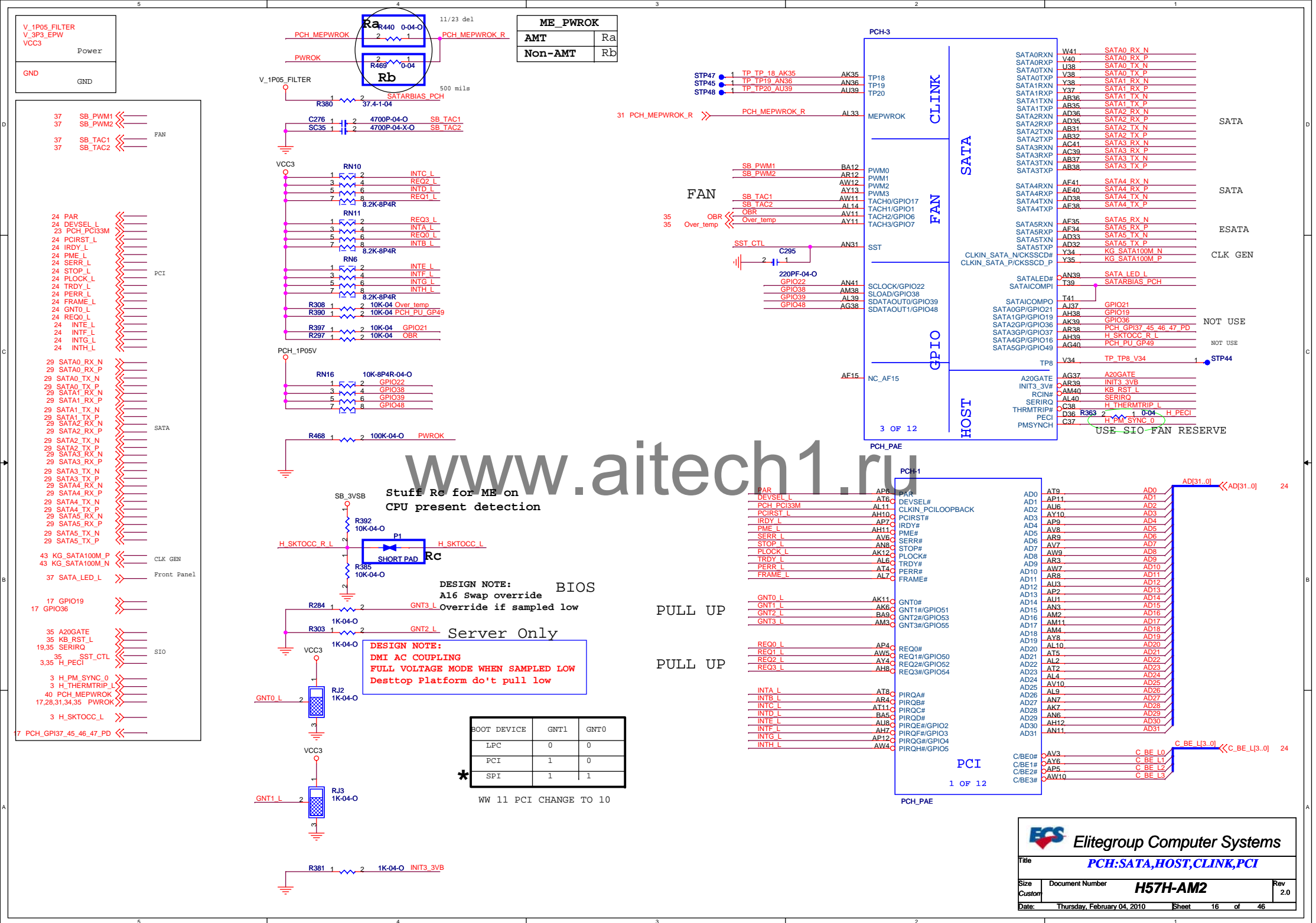
DDR3_DRAMRST_L 5,11,12,13

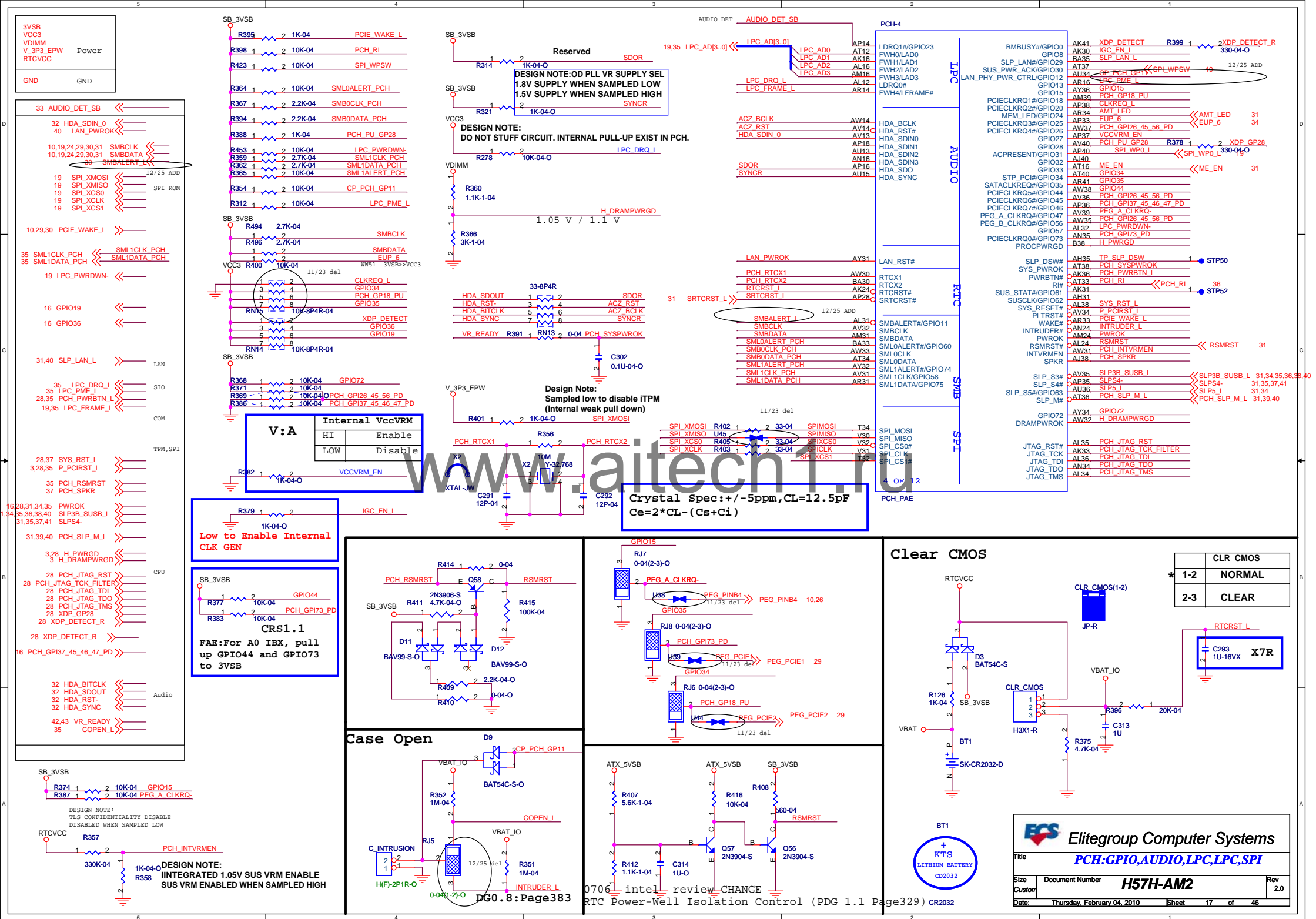


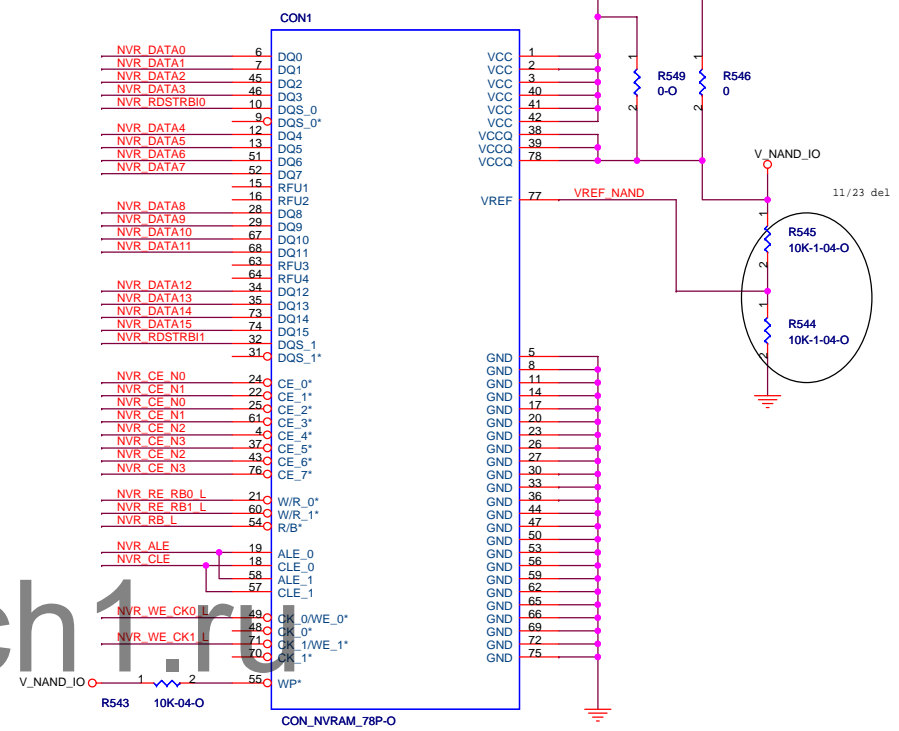
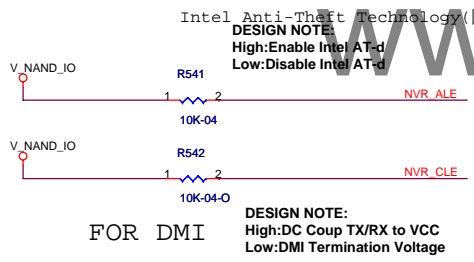
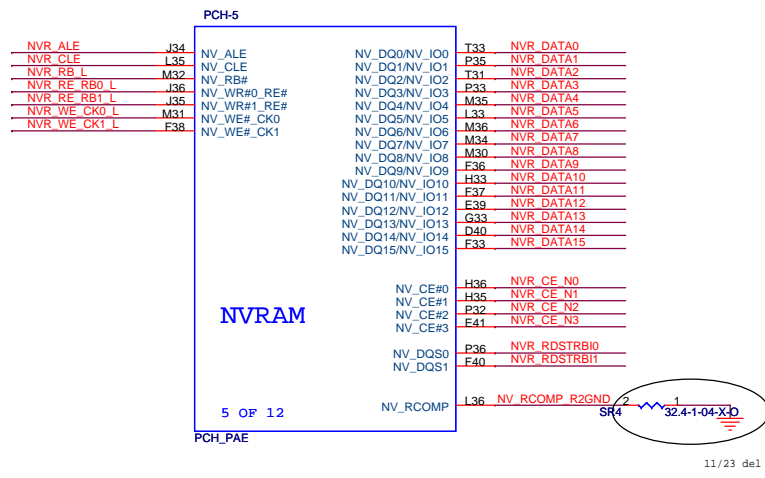
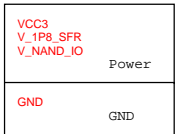
DDR_VTT	Power
VDIMM	
DIMM_VDDSPD	
GND	GND

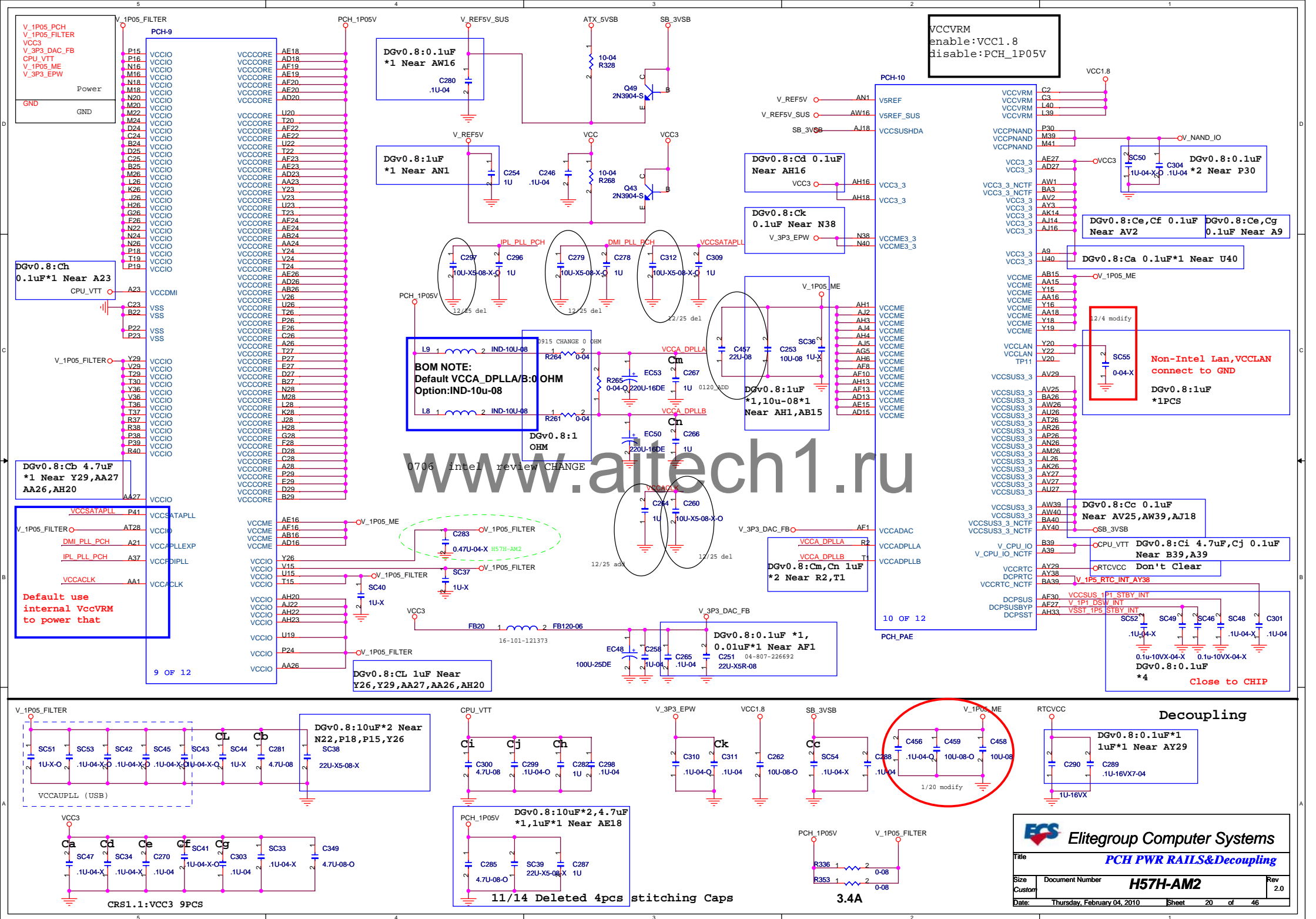
6.13 M3B_MA[15..0]
6.13 M3B_ODT[3..0]
6.13 M3B_CSB[3..0]
6.13 M3B_CKE[3..0]
6.13 M3B_BS[2..0]

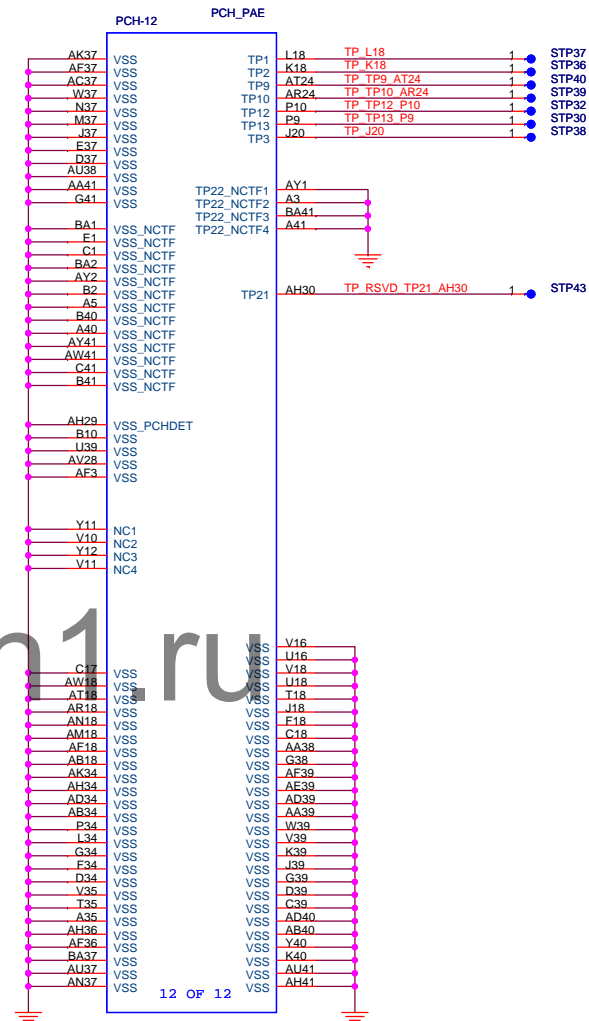
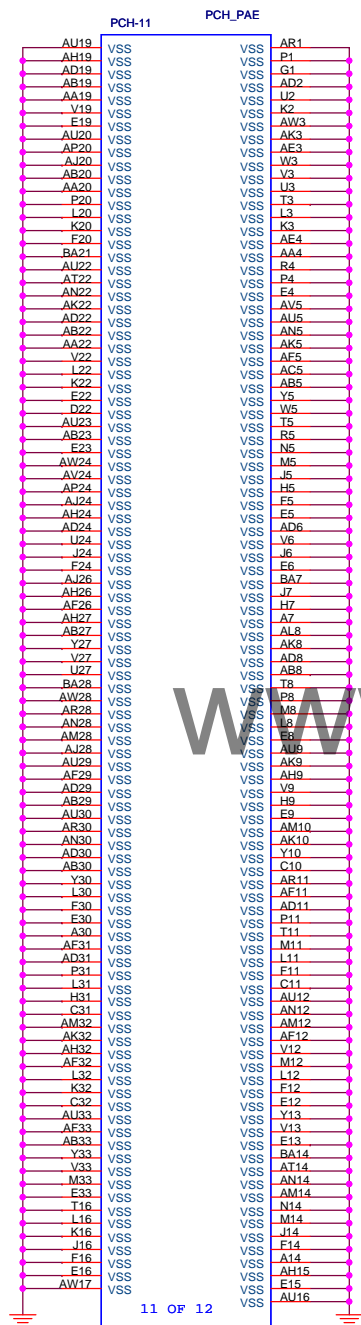


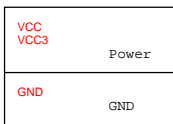






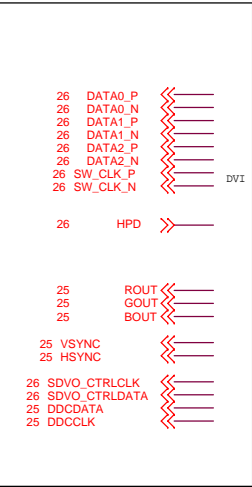




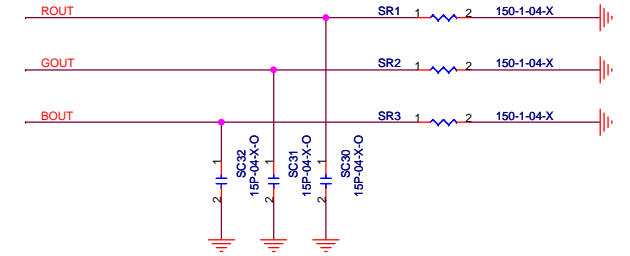
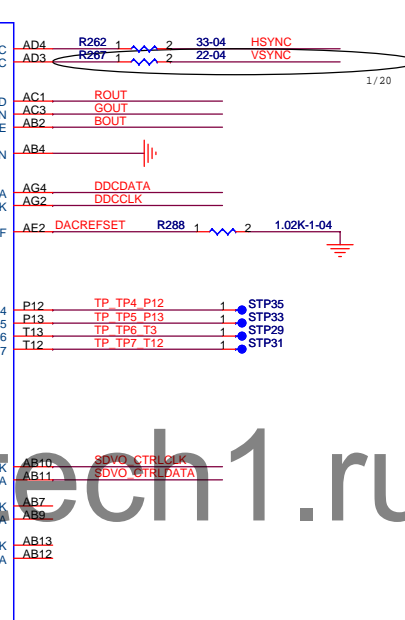
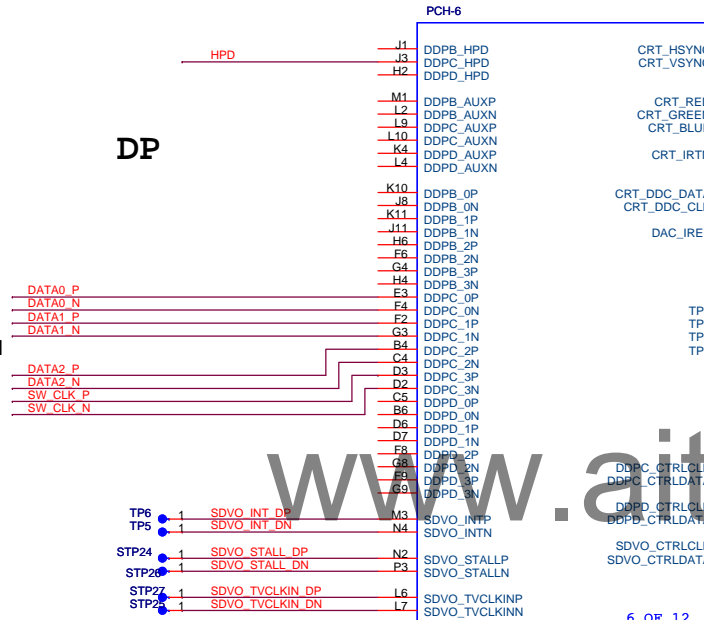


(WW07 DVI-I ONLY PORT B)

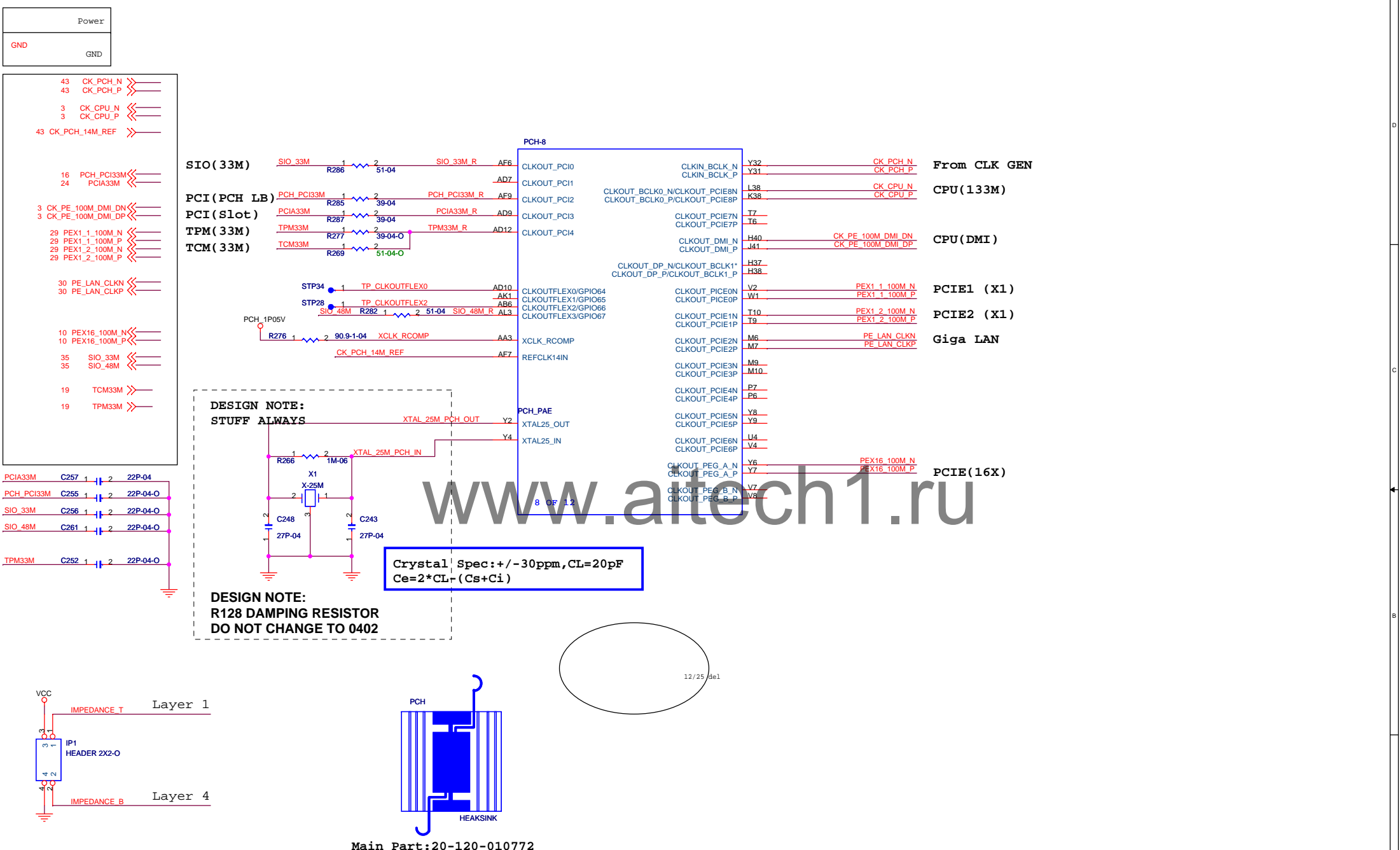
Port B: Capable of SDVO/HDMI/DVI/DP
Port C: Capable of HDMI/DVI/DP
Port D: Capable of HDMI/DVI/DP



Port C HDMI



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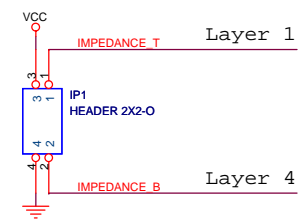
DESIGN NOTE:

STUFF ALWAYS

DESIGN NOTE:

**R128 DAMPING RESISTOR
DO NOT CHANGE TO 0402**

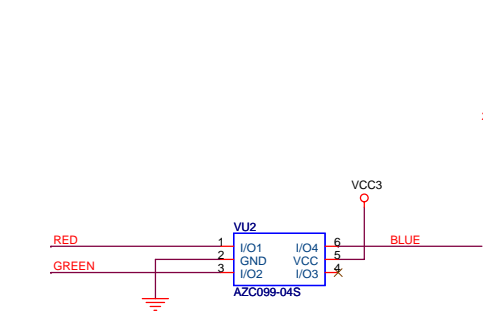
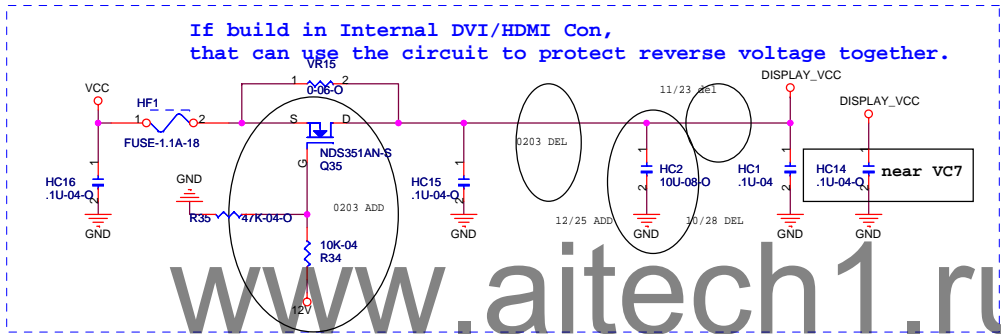
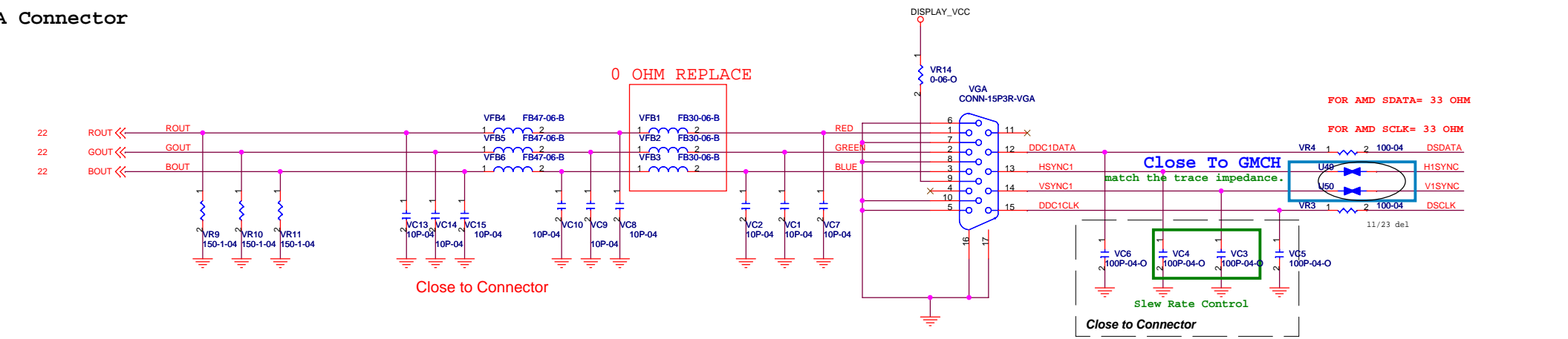
**Crystal Spec: +/- 30ppm, CL=20pF
Ce=2*CL/(Cs+Ci)**



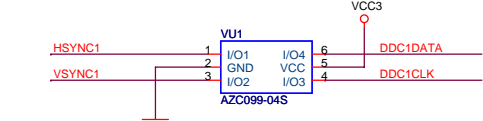
Main Part:20-120-010772

1080 : trace width 4 mil 50 ohm
Trace Length 3150 mils
Spacing: 1.clearance to itself 50/4/50(S:W:S)
2.clearance to other signal 3W

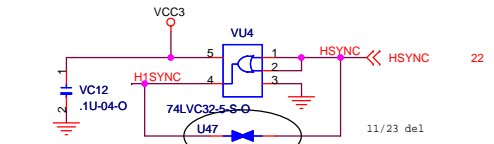
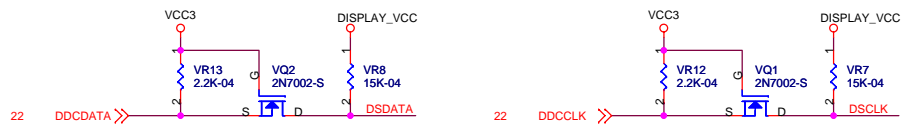
VGA Connector



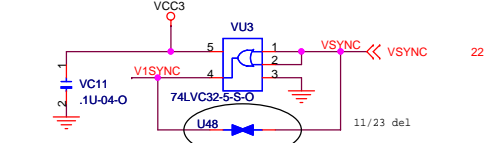
Close to Connector



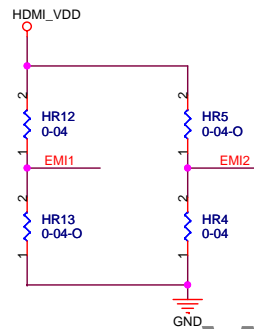
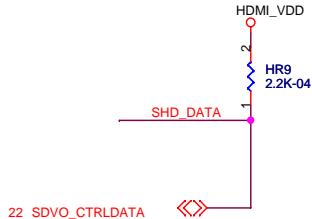
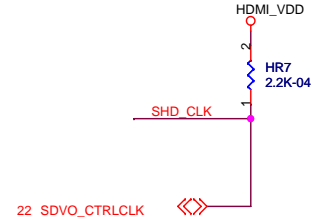
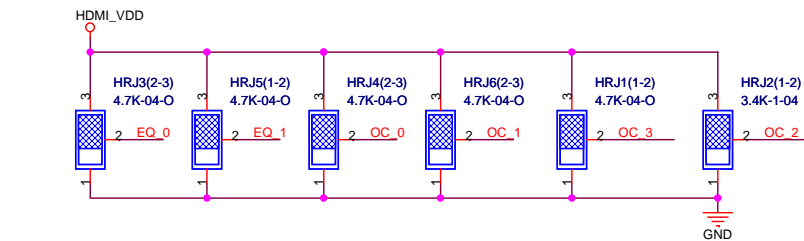
Close to Connector



FOR AMD RESERVE 74LVC32
PLEASE DOUBLE CHECK H/VSYNC OUTPUT VOLTAGE



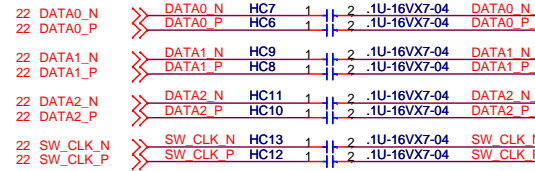
FOR AMD RESERVE 74LVC32
PLEASE DOUBLE CHECK H/VSYNC OUTPUT VOLTAGE



	PS8101	PI3VDP411LSTZDES
EQ_0	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
EQ_1	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_0	4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_1	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_2	499 1% OHM PULL DOWN	
OC_3	NC	

Level shifter noise issue

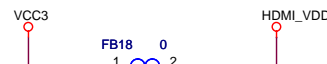
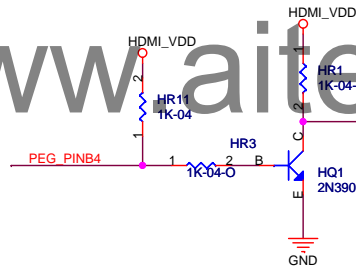
HDMI_VDD 1 2 SW_CLK_P C
HR14 1.5K-1-04-0



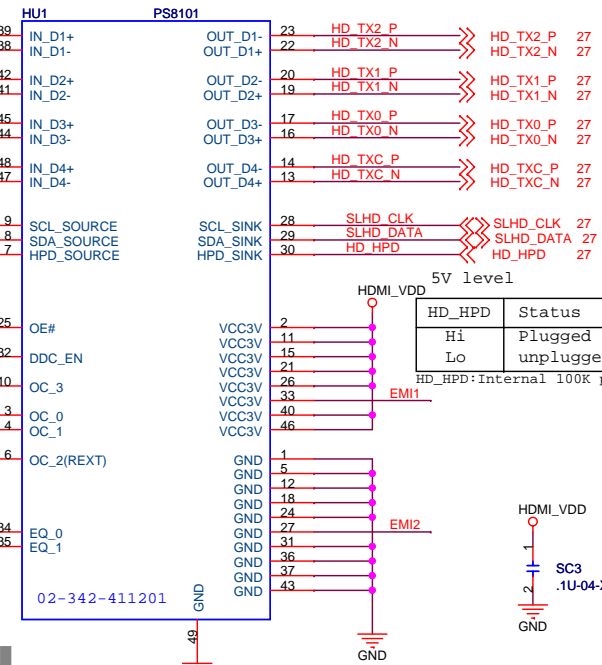
DDC_EN	Passgate
3.3V	Enable
0	Disable

22 HPD 3.3V level

10,17 PEG_PINB4



Level Shifter



OC_3	OC_2	OC_1	OC_0	Vswing (mV)	Pre/De-emphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0

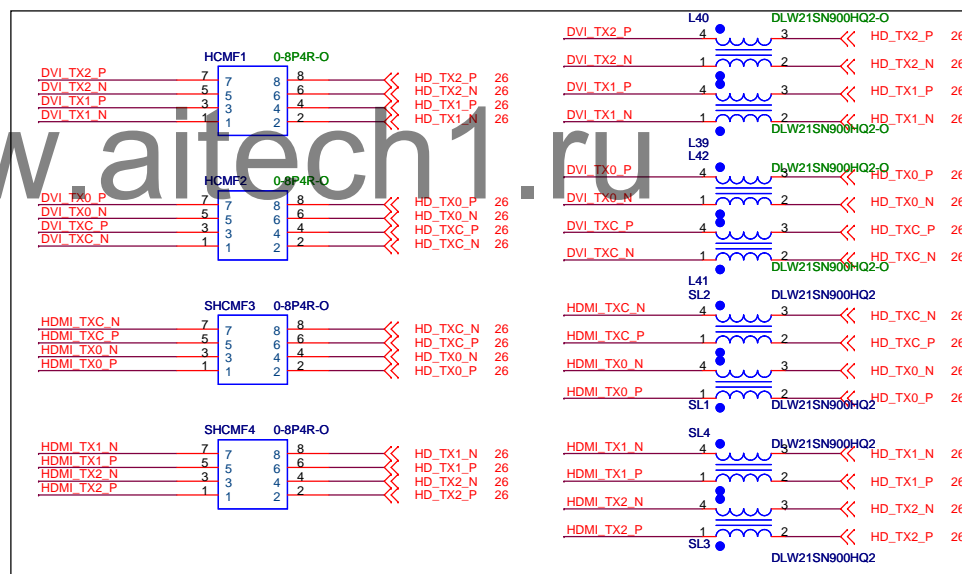
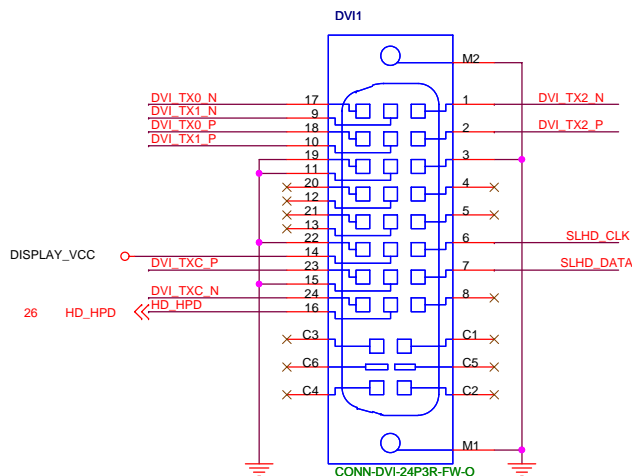
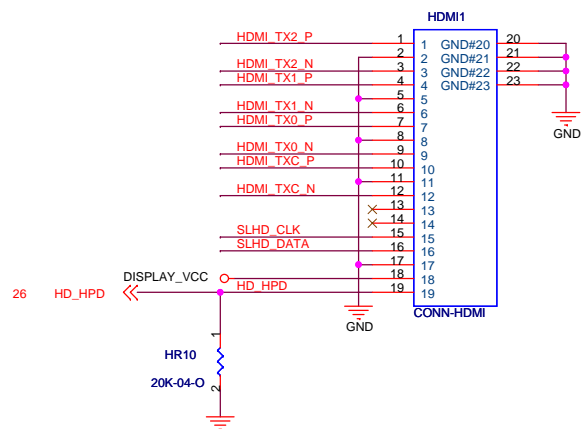
EQ_0	EQ_1	Equalization (dB)
0	0	3
0	1	7.2
1	0	10
1	1	20

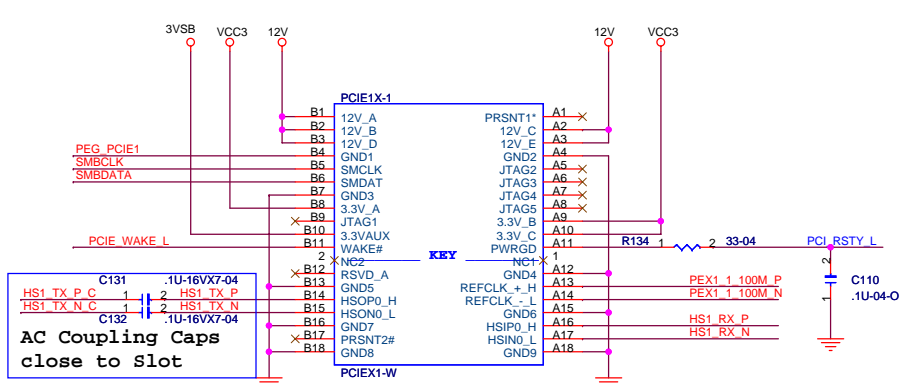
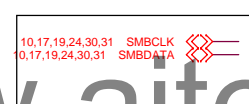
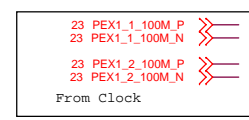
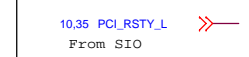
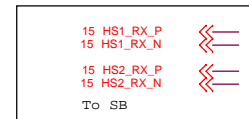
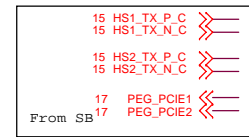
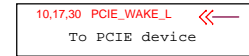
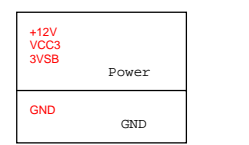
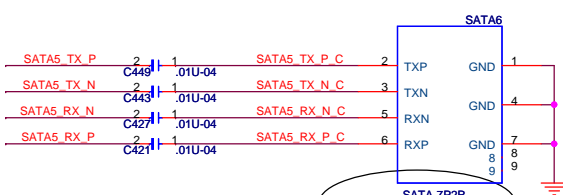
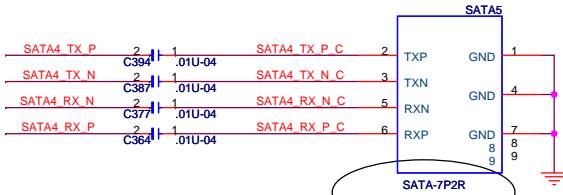
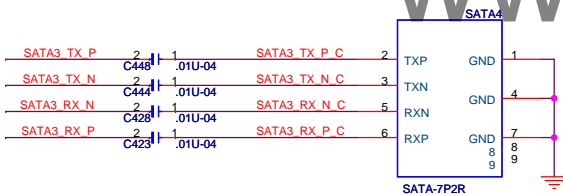
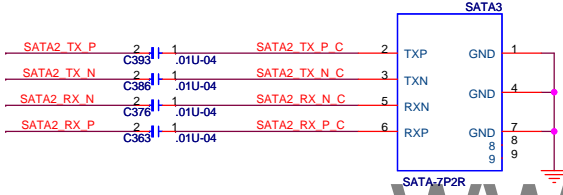
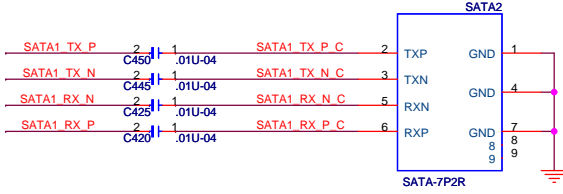
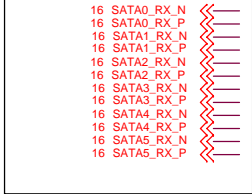
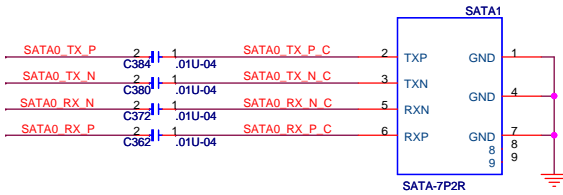
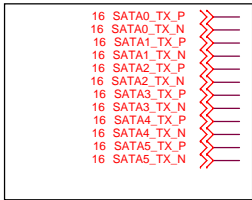
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Title: **HDMI Interface (optional)**

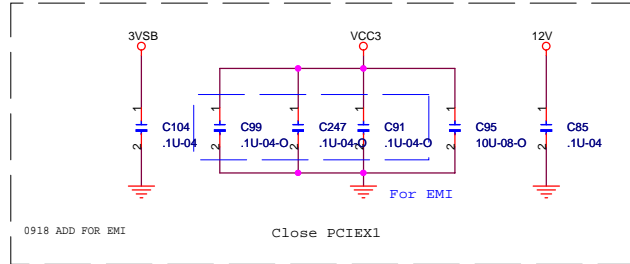
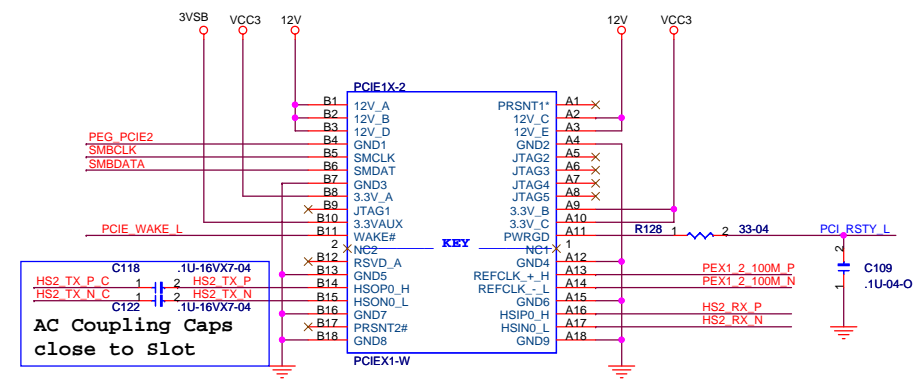
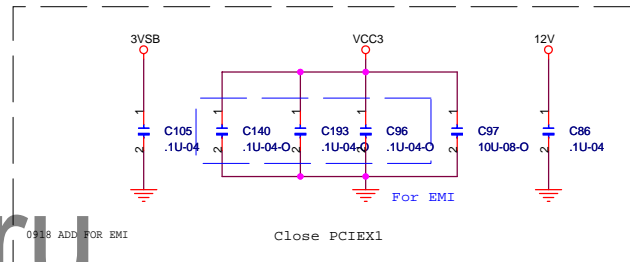
Size: Custom Document Number: **H57H-AM2** Rev: 2.0

Date: Thursday, February 04, 2010 Sheet: 26 of 46

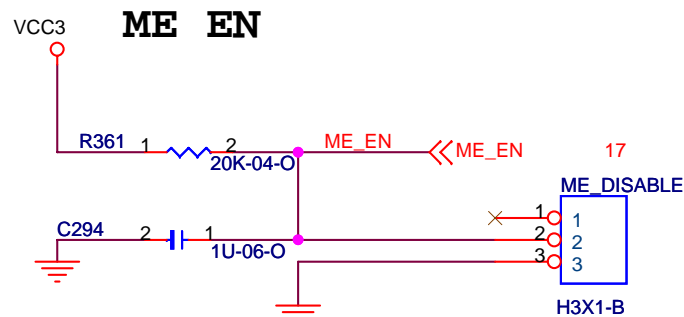
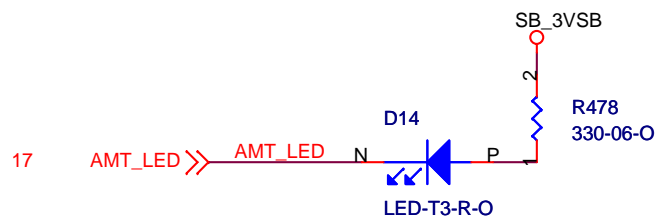




	PC_RST
INTEL	SIO:PCI REST
AMD	NB:PCIE REST
NV?	



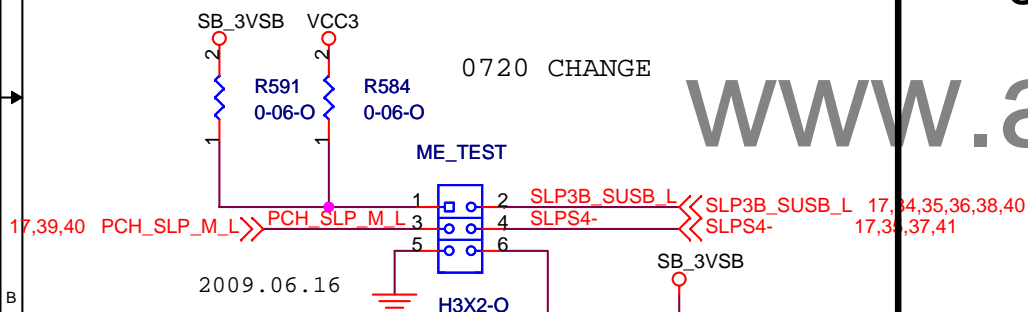
AMT_LED (optional)



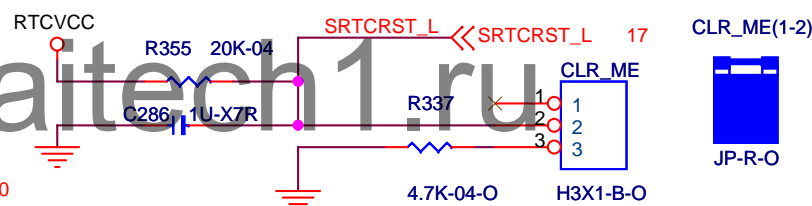
ME EN Clear Header

	ME EN
* 1-2	NORMAL
2-3	ME_DI

ME_TEST (optional)

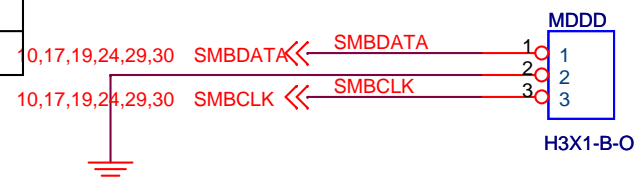


Clear ME (optional)



ME Clear Header

	CLR_ME
* 1-2	NORMAL
2-3	CLEAR ME



- 16,17,28,34,35 PWROK >> 1 STP41
- 17 RSMRST >> 1 STP53
- 17,40 SLP_LAN_L >> 1 TP1
- 16 PCH_MEPWROK_R >> 1 STP49
- 17,34 SLP5_L >> 1 STP46
- 17,39,40 PCH_SLP_M_L >> 1 TP4
- 17,34,35,36,38,40 SLP3B_SUSB_L >> 1 TP3
- 17,35,37,41 SLPS4- >> 1 STP51



Elitegroup Computer Systems

Title **AMT6.0 (optional)**

Size A Document Number

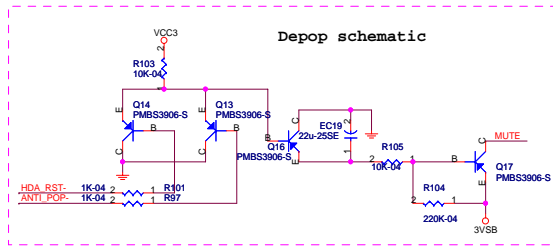
H57H-AM2

Rev 2.0

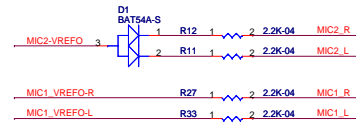
Date: Friday, February 05, 2010

Sheet 31 of 46

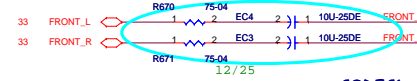
Depop schematic



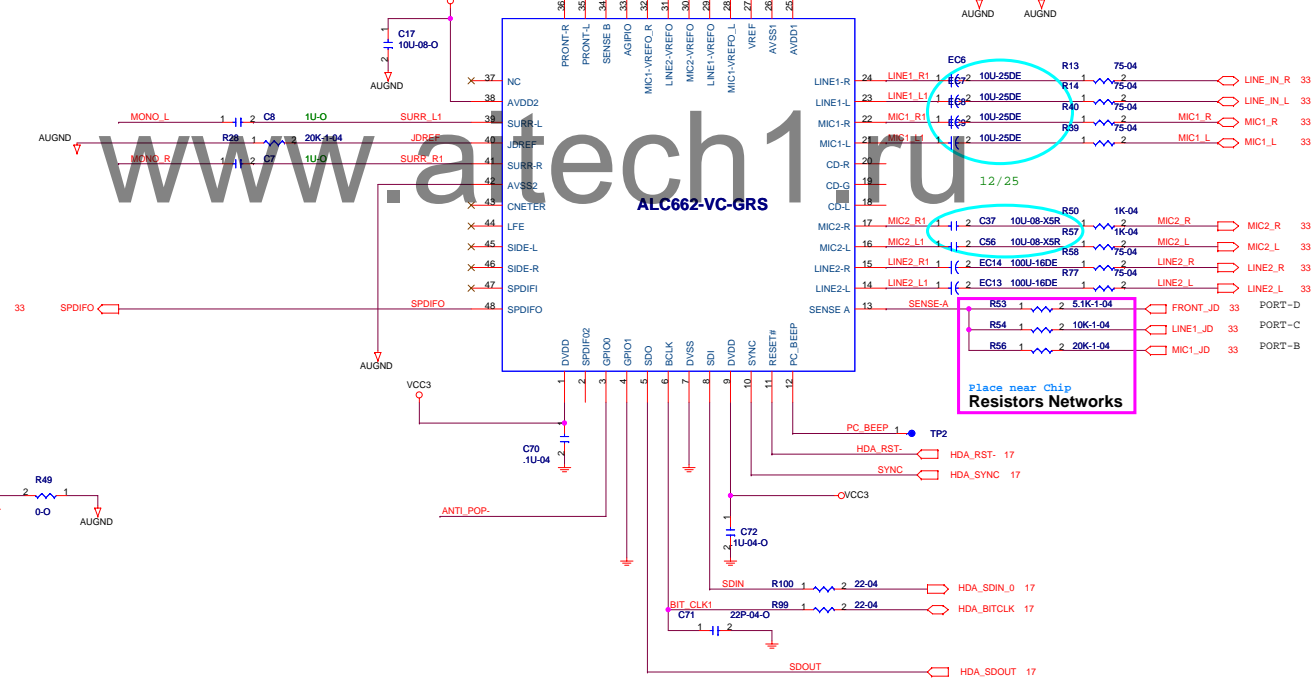
MIC Bias



Place near Chip Resistors Networks



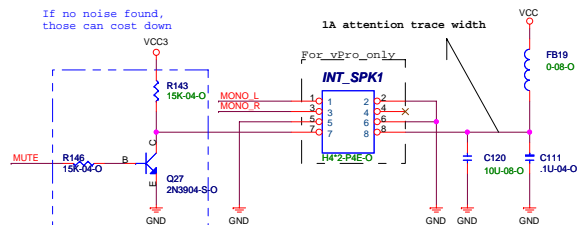
CODEC1

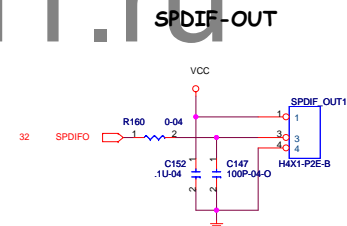
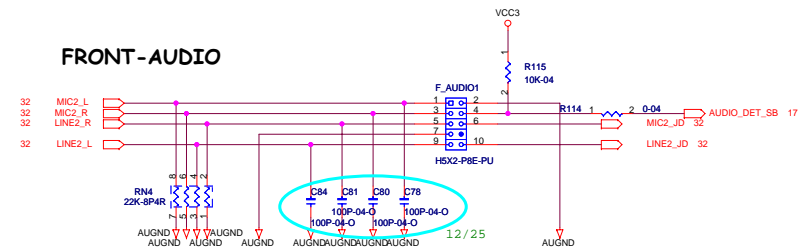
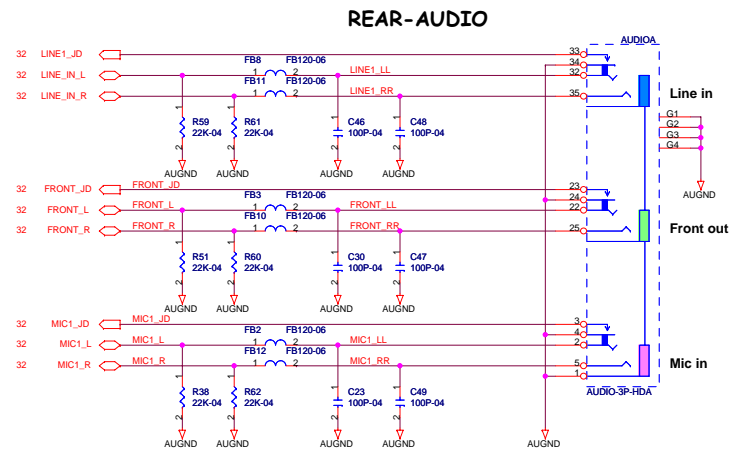


Place near Chip Resistors Networks

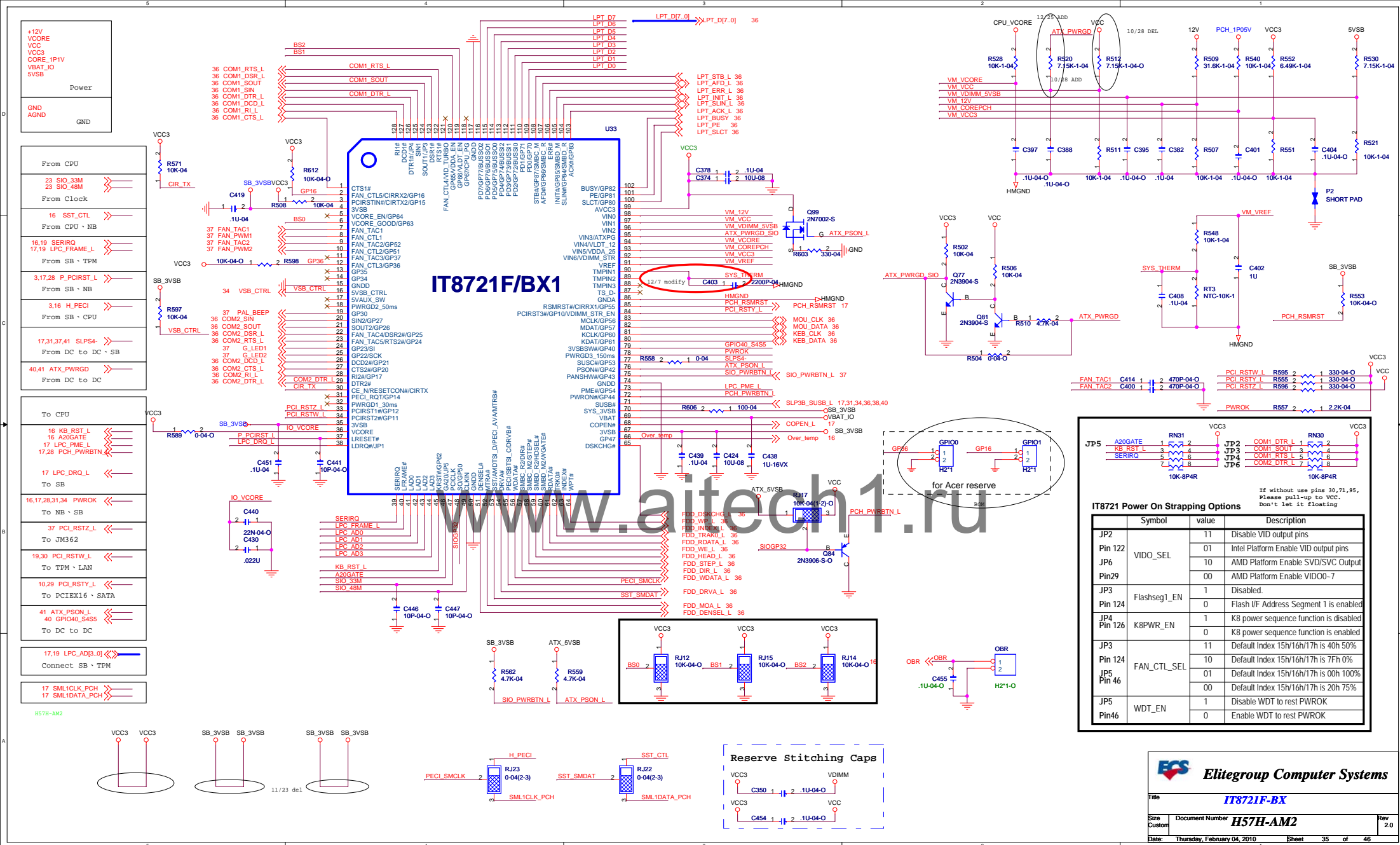


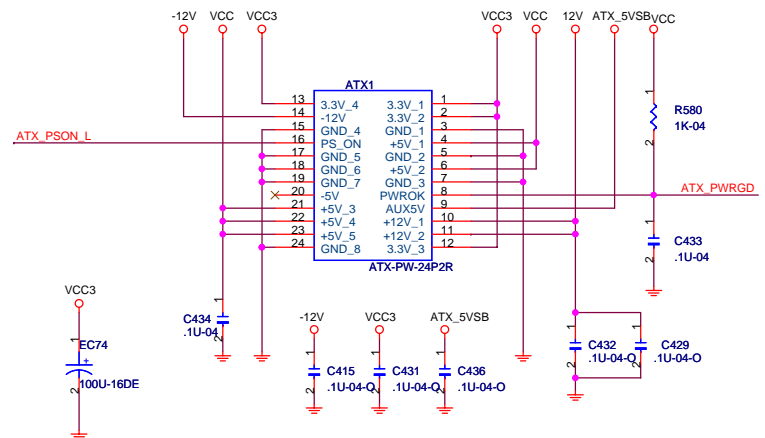
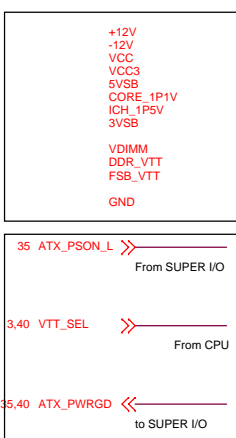
If no noise found,
those can cost down



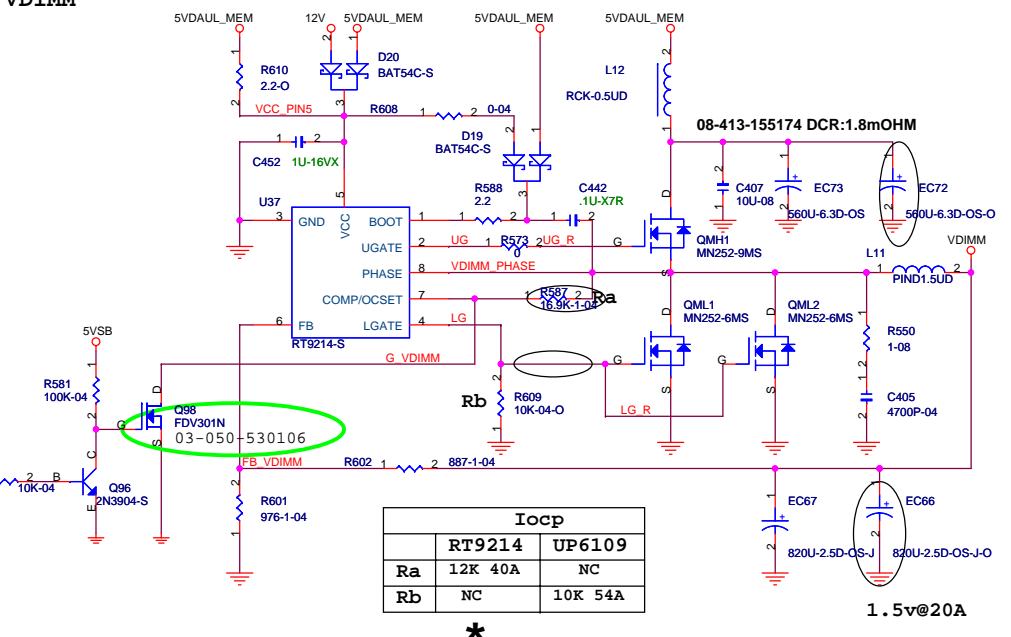


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VDIMM



VCC1.8

1.8V@1.5A

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DDR_VTT

DDR VTT~0.83A (DDR3)

PCH_1P05V

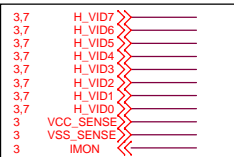
1.05V~1.1V@6.5A 1.05V~1.1V@3A Max

For Non-AMT

VREF25

Elitegroup Computer Systems
 Title DC-DC PCH Core,VDIMM,V_1P8_SFR
 Size Custom Document Number H57H-AM2 Rev 2.0
 Date: Thursday, February 04, 2010 Sheet 41 of 46

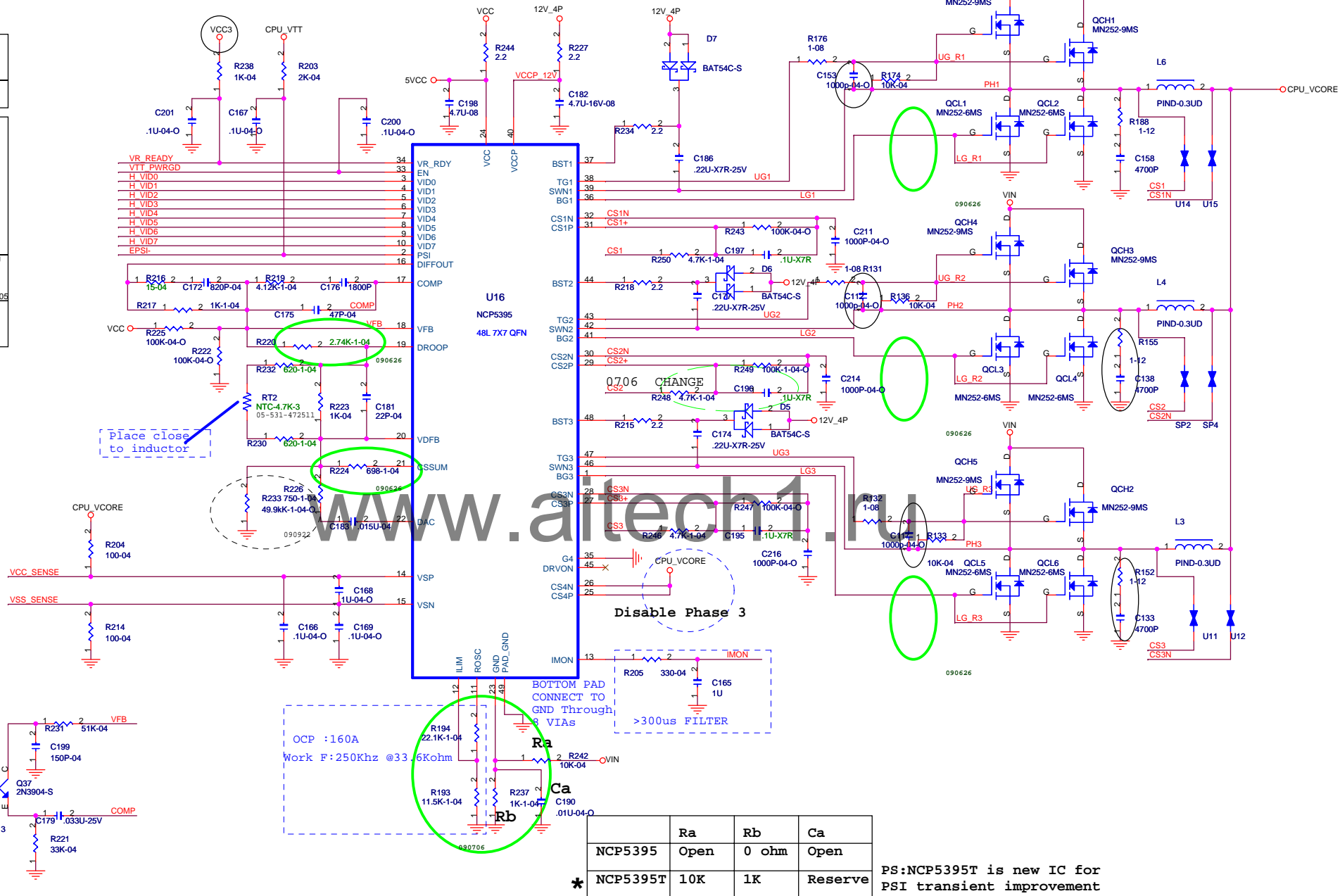
VCORE VCC CPU_VTT	POWER
GND	GND



	From CPU
--	----------

17,43 VR_READY <<————

3. ERSI-



	Ra	Rb	Ca
NCP5395	Open	0 ohm	Open
NCP5395T	10K	1K	Reserv

PS:NCP5395T is new IC for
PSI transient improvement

